

AN6354

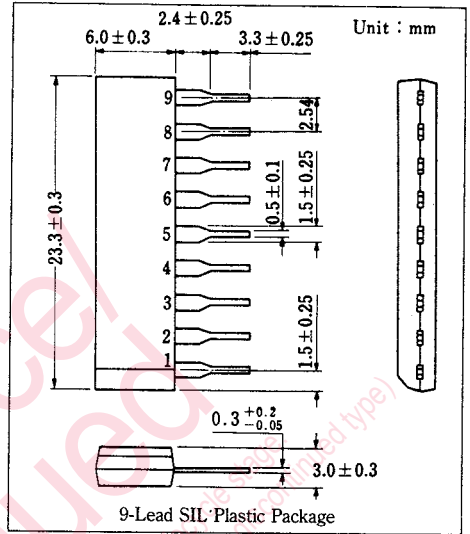
VTR 2H/4H/6H Automatic Discriminator

Outline

The AN6354 is an integrated circuit designed for VTR's 2H/4H/6H automatic discrimination.

Features

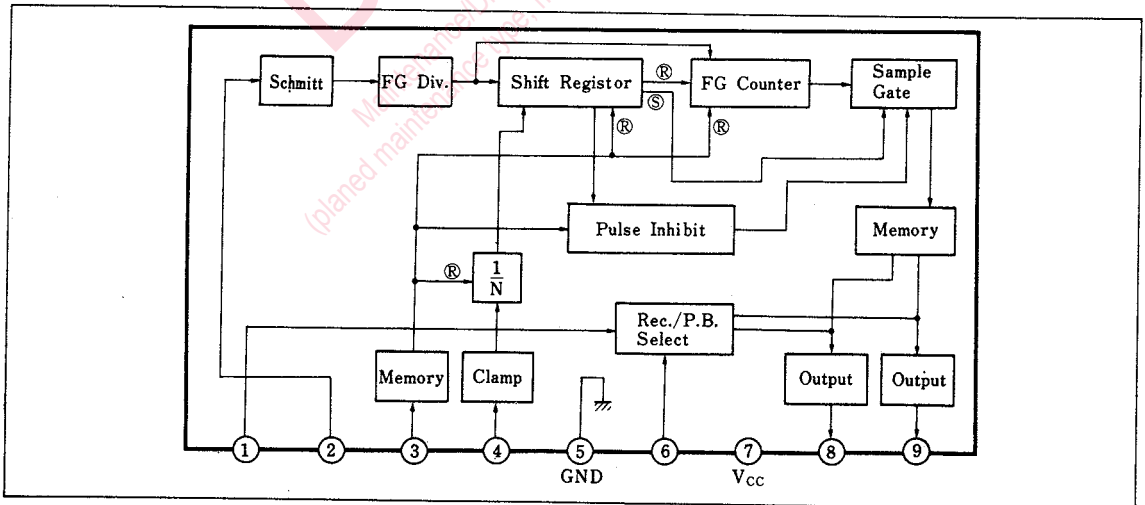
- The functions consist of:
 - FG divider
 - FG counter circuit
 - Memory circuit
- Supply voltage: 5V



Pin

Pin No.	Pin Name
1	Rec./P.B. Select
2	Cap. FG Input
3	Memory
4	P.B. CTL Input
5	GND
6	Rec. 2/4/6 Select
7	V _{cc}
8	B Output
9	A Output

Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

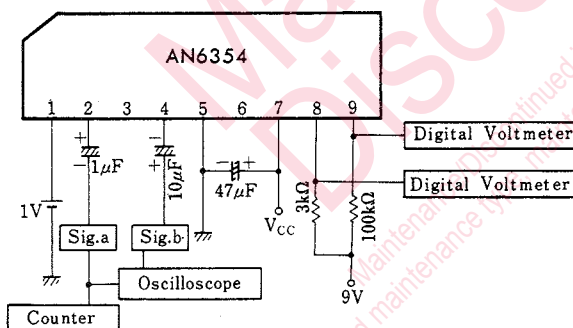
Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	6.0	V
Power dissipation (Ta=70°C)	P _D	100	mW
Operating ambient temperature	T _{opr}	-20~+70	°C
Storage temperature	T _{stg}	-55~+150	°C

■ Electrical Characteristics (V_{CC} = 5 V, Ta=25°C)

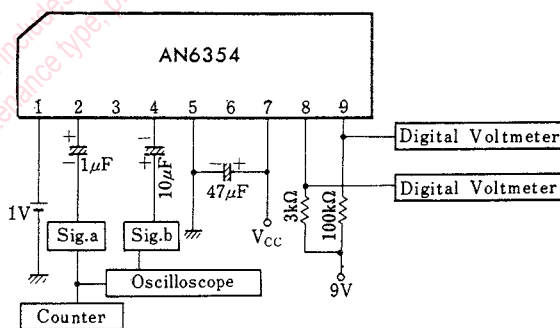
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
CAP. FG signal input sensitivity	S ₂	1		60			mV _{P-P}
PB CTL signal threshold voltage	V _{t4}	2		350			mV _{P-P}
A/B high-level output	V _{OHA, B}	3	100KΩ, 9 V to A/B output	8.4			V
A/B low-level output	V _{OLA, B}	3	3KΩ, 9 V to A/B output			0.4	V
Rec. (H) /P.B. (L) select sensitivity (Rec. mode)	S ₁	4		3.0			V
Memory ON (L) /OFF select sensitivity (memory ON)	S ₃	5				1.5	V
Rec.2/4/6 select (6H mode)	S ₆₍₆₎	6		0		1.0	V
Rec.2/4/6 select (4H mode)	S ₆₍₄₎	6		2.0		3.5	V
Rec.2/4/6 select (2H mode)	S ₆₍₂₎	6		4.5		5.0	V
Circuit current	I ₇	7	Without load	5		10	mA

Note) Operating supply voltage range V_{cc(opr)} = 4.5~5.5V

Test Circuit 1 (S₂)



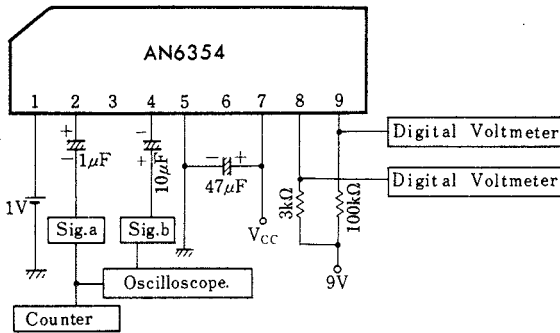
Test Circuit 2 (S₄)



- Sig.a) Input signal: Sine wave
f=1440Hz
- Sig.b) Input signal: Pulse
f=30Hz, 1V_{o-p}, Width 10 μ s
- P.B. 2H Mode
- ※ After setting a size of Sig.a) above input sensitivity (60mV_{p-p}) and confirming output logic of the Pins⑧ and ⑨ (2H mode) lower the size of Sig.a) and measure Sig.a) when the output logic enters the 4H mode(6H mode will do).

- Sig.a) Input signal: Sine wave
f=720Hz, 200mV_{p-p}
- Sig.b) Input signal: Pulse
f=30Hz, Width 10 μ s
- P.B. 4H Mode
- ※ After setting a size of Sig.b) above input sensitivity(350mV_{o-p}) and confirming output logic of the Pins⑧ and ⑨ (4H mode), lower the size of Sig.b) and measure Sig.b) when the logic of the Pins⑧ and ⑨ is changed to the 2H mode (forced 2H).

Test Circuit 3 (V_{OH} , V_{OL})

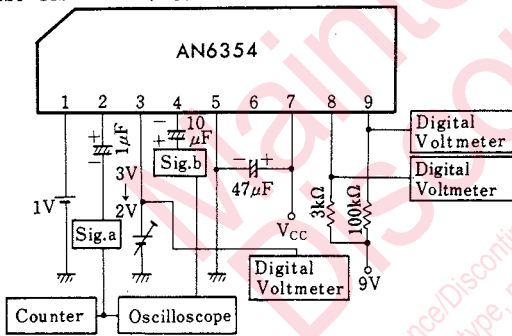


- Sig.a) Input signal: Sine wave
 $f=720\text{Hz}$, 200mV_{p-p}
- Sig.b) Input signal: Pulse
 $f=30\text{Hz}$, 1V_{o-p} , Width $10\mu\text{s}$
- P.B. 4H Mode

※ Measure the level (logic) of the Pins⑧ and ⑨ with a digital voltmeter.

Pin⑧ (A) . . . High } 4H Mode
Pin⑧ (B) . . . Low }

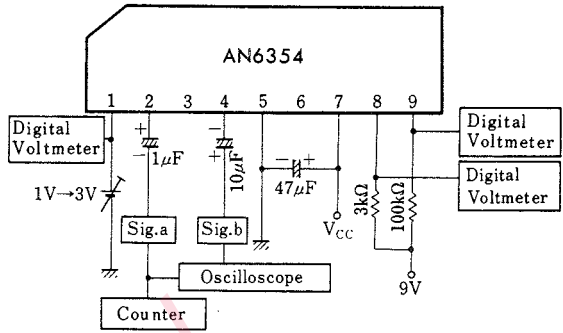
Test Circuit 5 (S_3)



- Sig.a) Input signal: Sine wave
 $f=720\text{Hz}, (1440\text{Hz})$ 200mV_{p-p}
- Sig.b) Input signal: Pulse
 $f=30\text{Hz}$, 1V_{o-p} , Width $10\mu\text{s}$
- P.B. 4H Mode

※ After setting a Pin③ voltage to 3V and confirming that a frequency for Sig.a) is 720Hz and the output logic of the Pins⑧ and ⑨ is the 4H mode, lower a Pin③ voltage to 3V-2V. Then, set the frequency for Sig.a) to 1,440Hz(2H mode) and measure a Pin③ voltage with a digital voltmeter when the logic of the Pins⑧ and ⑨ is not in the 2H mode.

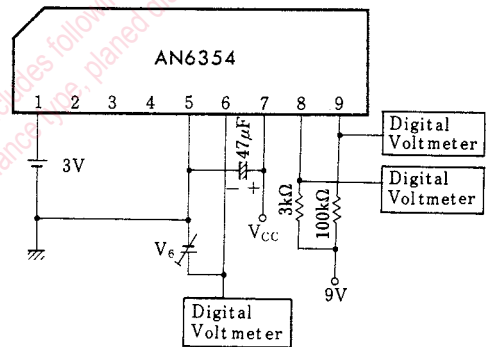
Test Circuit 4 (S_1)



- Sig.a) Input signal: Sine wave
 $f=480\text{Hz}$, 200mV_{p-p}
- Sig.b) Input signal: Pulse
 $f=30\text{Hz}$, 1V_{o-p} , Width $10\mu\text{s}$
- P.B. 6H Mode
- Rec. 2H Mode

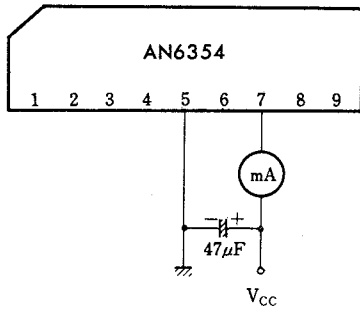
※ Change a Pin① voltage to 1V-3V, and measure with a digital voltmeter the Pin① voltage when the output logic of the Pins⑧ and ⑨ are changed from the 6H mode(PB) to 2H mode(Rec.).

Test Circuit 6 ($S_{6(6)}$, $S_{6(4)}$, $S_{6(2)}$)



- Rec. select sensitivity(6H/4H)
- Change a Pin⑥ voltage to 1V-2V, and measure with a digital voltmeter the Pin⑥ voltage when the output logic of the Pins ⑧ and ⑨ is changed from the 6H mode to the 4H mode.
- Rec. select sensitivity(4H/2H)
- Change a Pin⑥ voltage to 3.5V-4.5V, and measure with a digital voltmeter the Pin⑥ voltage when the output logic of the Pins ⑧ and ⑨ are changed from the 4H mode to the 2H mode.

Test Circuit 7 (I₇)



※ Measure a supply current when Vcc is impressed to the Pin⑦ in a no-load state.

■ Precautions for Use

- For PAL use Although there are two outputs such as Pin⑧ (B/output) and Pin⑨ (A/output), use the Pin⑨ (Aoutput) only.
- PB automatic select sensitivity (CTL frequency=25Hz)

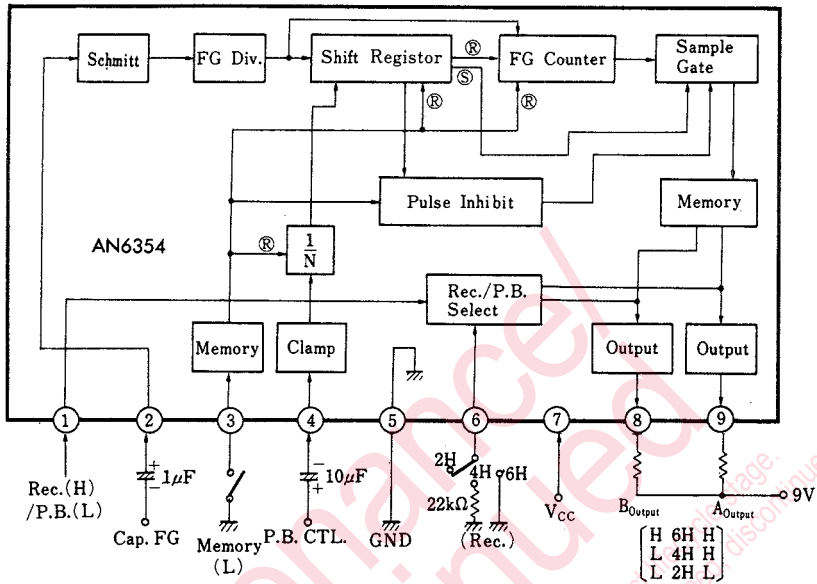
FG Freq.[Hz]	240	480	505	720	960	1010	1200	1440	1680	1920
Mode	Unchanged	6 H			3 H			Forced 3 H		
Output logic	A	H			L			L		

- Relations between FG and PB CTL
 ·FG output is a half frequency of FG(belt system).

	NTSC			PAL		
	2 H	4 H	6 H	3 H	6 H	
FG output frequency [Hz]	720	360	240	600	300	
P. B. CTL [Hz]	30	30	30	25	25	
FG Output/P. B CTL	24	12	8	24	12	
(FG Output/P. B. CTL) × 8	192	96	64	192	96	
Threshold value	128		80	128		
Output	A	L	H	H	L	H
	B	L	L	H		

- To discriminate 3H/6H in the PAL, use a threshold value "128" which discriminates 2H/4H in the NTSC.
- Since A/output changes only during 2H/4H in the NTSC, discriminate 3H/6H with A/output only in the PAL.

■ Application Circuit



Maintenance/Discontinued includes following four Product type (discontinued type)
 (planned maintenance type, maintenance type, planned discontinued type, discontinued type)

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