M50199P

DIGITAL DELAY

DESCRIPTION

The M50199P is a digital delay IC fabricated with silicon-gate CMOS technology.

The M50199 converts an input analog signal to a digital signal and writes to a memory IC. After a delay it reads out the digital signal from the memory IC and then converts to an analog signal again.

Lower noise and distortion delay signal is obtained by M50199P than by BBD. An A-D, D-A converter block formed of ADM (Adaptive Delta Modulation) circuit can produce a low cost delay system.

FEATURES

- Low noise (−90dBV typ)
  Low distortion (0.5 % typ)
- 3 mode delay time (15, 23, 30msec)

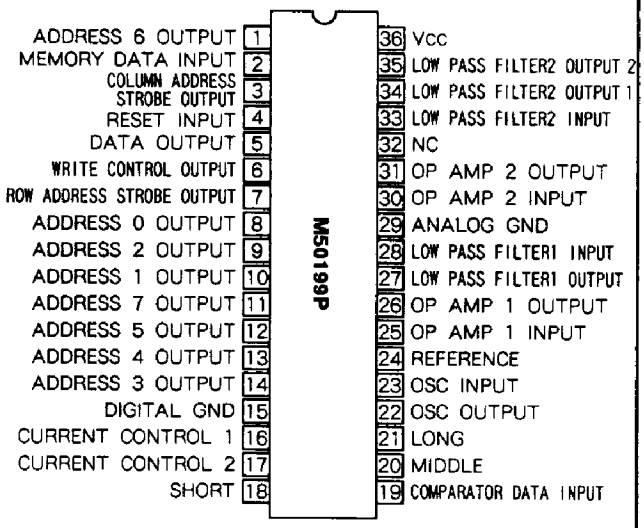
APPLICATION

AV surround, Electronic instrument

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ..... 4.0~5.5V
Rated supply voltage 5V

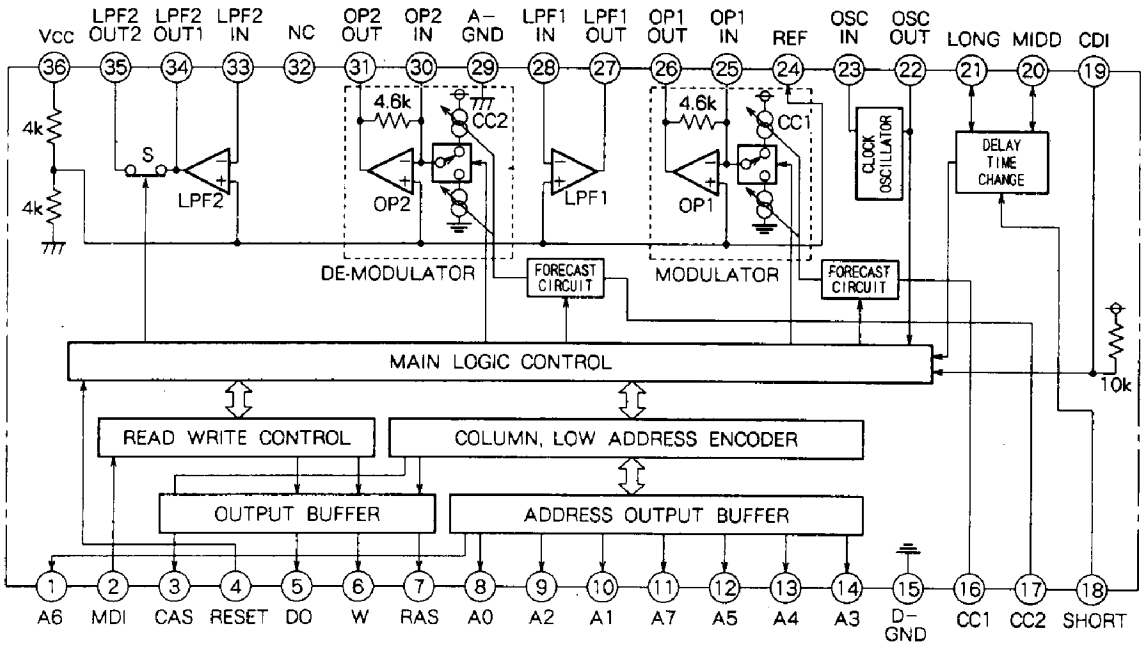
PIN CONFIGURATION (TOP VIEW)



Outline 36P4E

NC : NO CONNECTION

BLOCK DIAGRAM



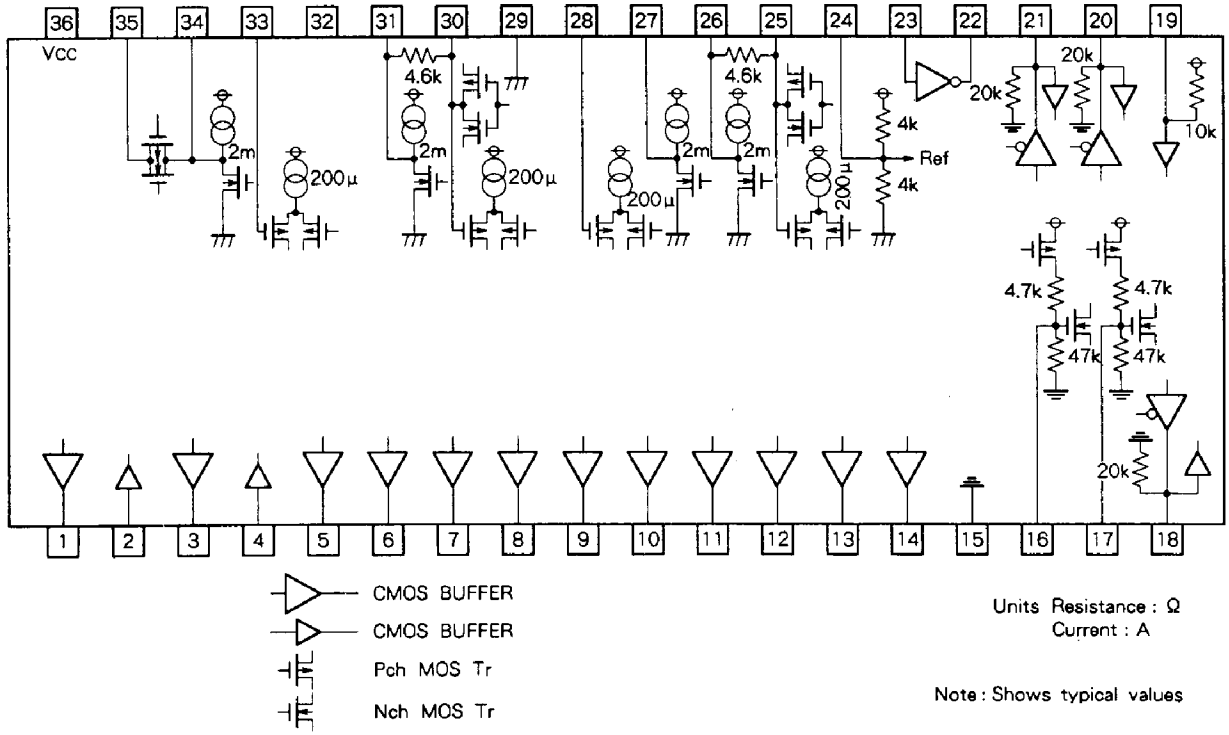
Unit Resistance : Ω

MITSUBISHI ELECTRIC

IN FUNCTIONS

Function	Symbol	Function outline
Reference voltage generator	REF	Generates reference voltage of analog circuit (1/2Vcc)
Low pass filter	LPF1, LPF2	Cuts unneccessary high frequency noise
Adaptive delta modulator	OP1, CC1	Converts analog signal to digital signal
Adaptive delta demodulator	OP2, CC2	Converts digital signal to analog signal
Forecast circuit		Makes the ADM operate best suited then improves S/N ratio and distortion
Clock generator circuit		Generates master clock typical frequency fcK = 3.27MHz
Change to delay time switch		Delay time 3modes can be selected (SHORT = 15 msec, MIDD = 23msec, LONG = 30 msec)
Switch	S	Turns on at SHORT, MIDD mode
Main control logic		Controls ADM circuits, delay time and memory IC
Read/write control		Controls read or write to memory IC
Row column address encoder		Selects address of the memory IC
Output buffer Address output buffer		Drives memory IC

I/O INTERFACE



PIN DESCRIPTION

No.	Name	Symbol	Function	Typical output DC voltage
①	ADDRESS 6 OUTPUT	A6	Connects to A6 (Address input 6) terminal of memory IC	5VP-O
②	MEMORY DATA INPUT	MD1	Connects to Q (Data input) terminal of memory IC	–
③	COLUMN ADDRESS STROBE OUTPUT	CAS	Connects to CAS (Column Address Strobe input) terminal of memory IC	5VP-O
④	RESET INPUT	RESET	Reset at the Low level	–
⑤	DATA OUTPUT	DO	Connects to D (Data input) terminal of memory IC	5VP-O
⑥	WRITE CONTROL OUTPUT	W	Connects to W (Write control input) terminal of memory IC	
⑦	ROW ADDRESS STROBE OUTPUT	RAS	Connects to RAS (Row Address Strobe input) terminal of memory IC	
⑧	ADDRESS 0 OUTPUT	A0	Connects to A0 terminal of memory IC	
⑨	ADDRESS 2 OUTPUT	A2	Connects to A2 terminal of memory IC	
⑩	ADDRESS 1 OUTPUT	A1	Connects to A1 terminal of memory IC	
⑪	ADDRESS 7 OUTPUT	A7	Connects to A7 terminal of memory IC	
⑫	ADDRESS 5 OUTPUT	A5	Connects to A5 terminal of memory IC	
⑬	ADDRESS 4 OUTPUT	A4	Connects to A4 terminal of memory IC	
⑭	ADDRESS 3 OUTPUT	A3	Connects to A3 terminal of memory IC	
⑮	DIGITAL GND	D – GND	Connects to analog GND at one point	0V
⑯	CURRENT CONTROL 1	CC1		0.7V Quiescent
⑰	CURRENT CONTROL 2	CC2		
⑱	SHORT	SHORT	Delay time Td = 15msec, output current for indicator Io = 5mA typ	5V(S) 0V(M, L)
⑲	COMPARATOR DATA INPUT	CD1	Connects to comparator output	–
⑳	MIDDLE	MIDD	Delay time Td = 23 msec, output current for indicator Io = 5mA typ	5V(M) 0V(S, L)
㉑	LONG	LONG	Delay time Td = 30 msec, output current for indicator Io = 5mA typ	5V(L) 0V(S, M)
㉒	OSC OUTPUT	OSC OUT	Connects to 3.27MHz ceramic filter	5VP-O
㉓	OSC INPUT	OSC IN	Connects to 3.27MHz ceramic filter or inputs external clock	–
㉔	REFERENCE	REF	≒ 1/2Vcc	2.5V
㉕	OP AMP 1 INPUT	OP1 IN	Forms integrator with external C	2.5V
㉖	OP AMP 1 OUTPUT	OP1 OUT		2.5V
㉗	LOW PASS FILTER 1 OUTPUT	LPF1OUT	Forms second order low pass filter with external C,R	2.5V
㉘	LOW PASS FILTER1 INTPUT	LPF 1IN		2.5V
㉙	ANALOG GND	A – GND		0V
㉚	OP AMP 2 INPUT	OP2 IN	Forms integrator with external C	2.5V
㉛	OP AMP 2 OUTPUT	OP2 OUT		2.5V
㉜	N. C.	NC		–
㉝	LOW PASS FILTER2 INTPUT	LPF2 IN	Forms second order low pass filter with external C,R	2.5V
㉞	LOW PASS FILTER 2 OUTPUT1	LPF2 OUT1		2.5V
㉟	LOW PASS FILTER 2 OUTPUT2	LPF2 OUT2		2.5V
㊱	Vcc	Vcc	Supply voltage 4~5.5V (5V typ)	–

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		7	V
I_{CC}	Circuit current		70	mA
P_d	Power dissipation		1100	mW
T_{opr}	Operating temperature		−20～+75	℃
T_{stg}	Storage temperature		−40～+125	℃

RECOMMENDED OPERATING CONDITIONS

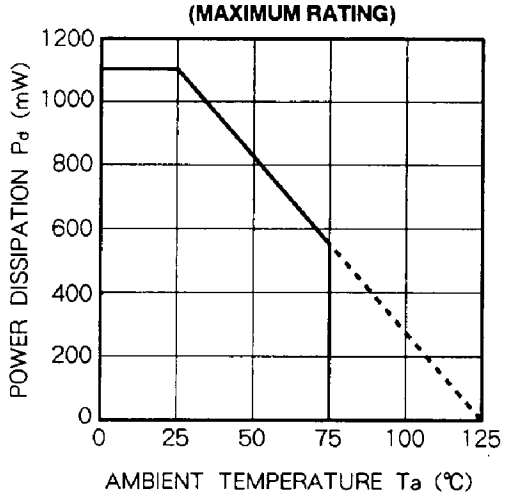
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	5.5	V
f_{ck}	Clock frequency			3.27	4.5	MHz
V_{IH}	High input voltage	MD1, Reset, CD1, SHORT, MIDD, LONG	$V_{CC}\times0.8$	V_{CC}	V_{CC}	V
V_{IL}	Low input voltage	MD1, Reset, CD1	0	0	$V_{CC}\times0.2$	V
CM	Load capacitance	A0～A7, RAS, CAS, DO, W			10	pF

ELECTRICAL CHARACTERISTICS (Ta = 25℃, unless otherwise noted)

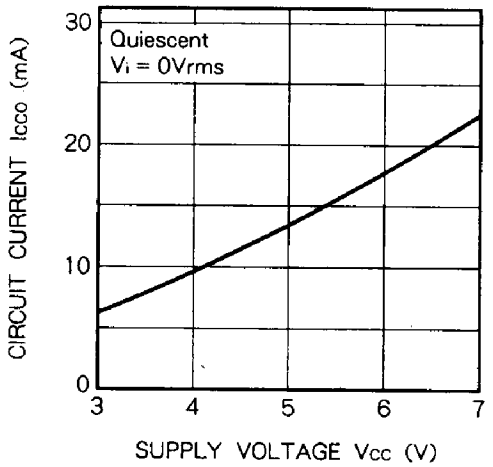
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
I_{CCO}	Circuit Current	Quiescent		8	15	25	mA
G_{VS}	Voltage gain	SHORT		−4.1	−2.6	−1.1	dB
G_{VM}		MIDD		−4.1	−2.6	−1.1	dB
G_{VL}		LONG		−4.1	−2.6	−1.1	dB
T_{dS}	Delay time	SHORT			15		ms
T_{dM}		MIDD			22.5		ms
T_{dL}		LONG			30		ms
V_{Omax}	Maximum output voltage	SHORT	THD = 3%	0.7	1.0		Vrms
		MIDD, LONG					
THD	Output distortion	SHORT Vo = 200mVrms			0.6	1.5	%
No	Output noise voltage	SHORT	Rg = 50 Ω DIN-AUDIO		−91	−74	dBV
		MIDD, LONG			−90	−74	
SVRR	Supply voltage rejection ratio	△Vcc = − 20dBv, 100Hz			−40	−25	dB

TYPICAL CHARACTERISTICS

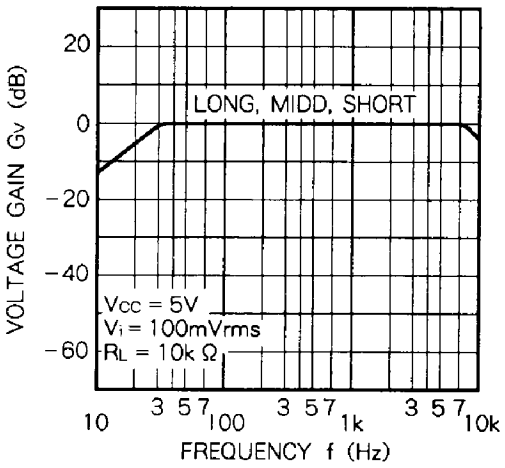
THERMAL DERATING (MAXIMUM RATING)



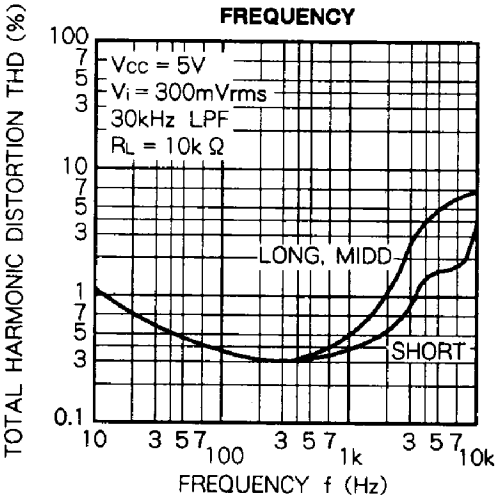
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



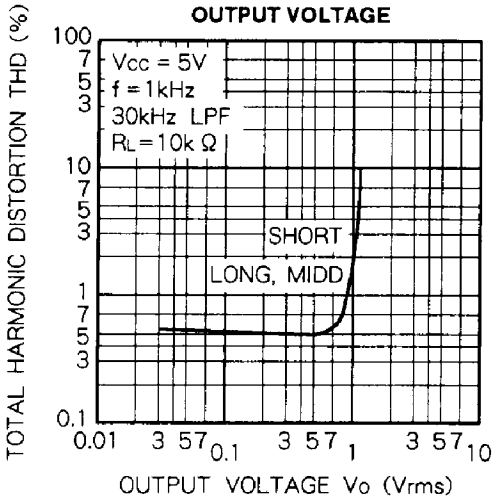
VOLTAGE GAIN VS. FREQUENCY



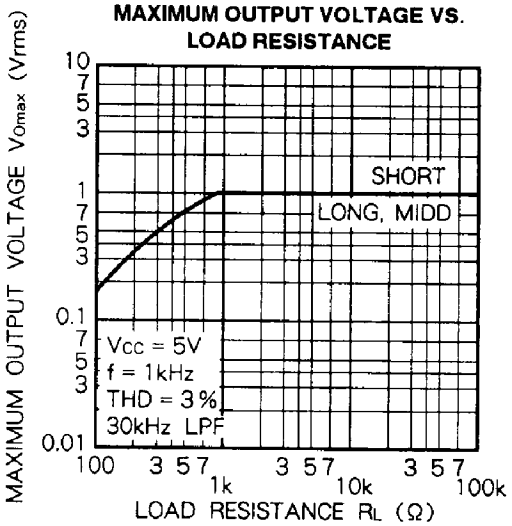
TOTAL HARMONIC DISTORTION VS. FREQUENCY



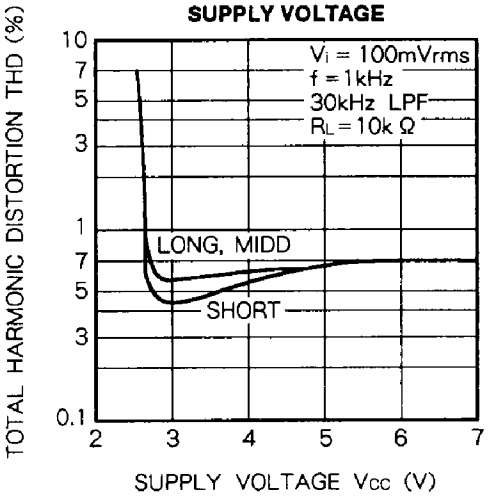
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE



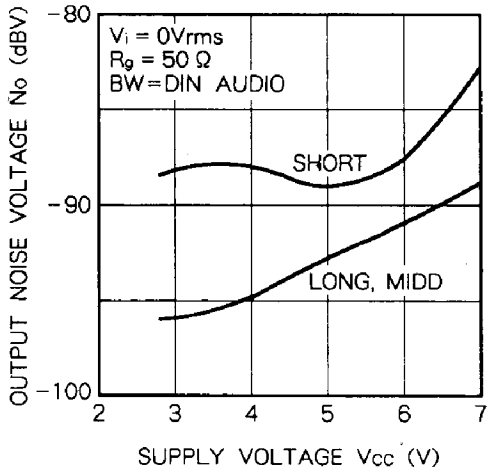
MAXIMUM OUTPUT VOLTAGE VS. LOAD RESISTANCE



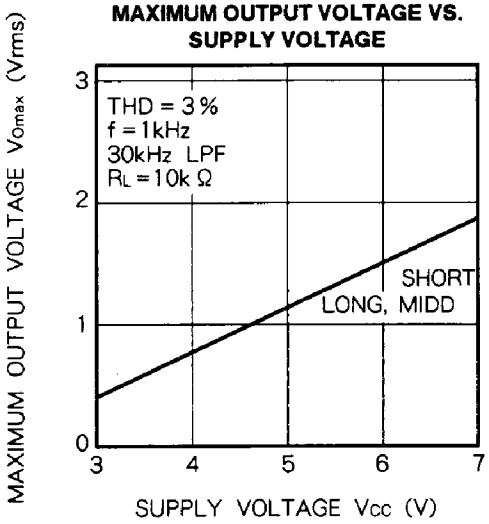
TOTAL HARMONIC DISTORTION VS. SUPPLY VOLTAGE



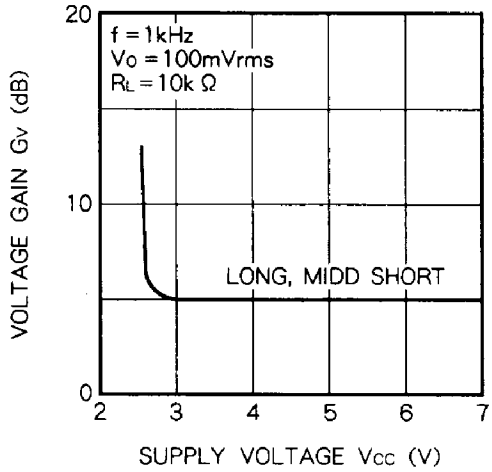
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



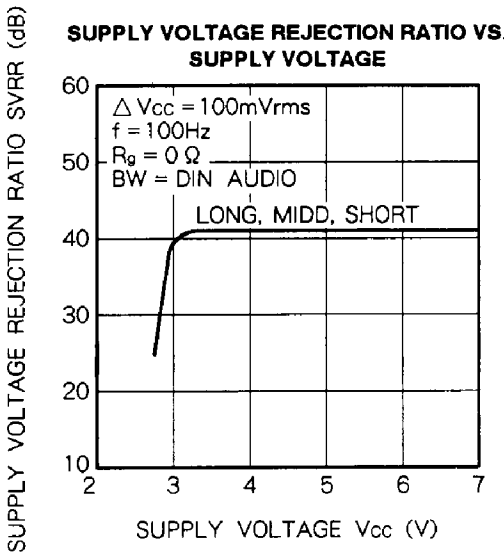
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



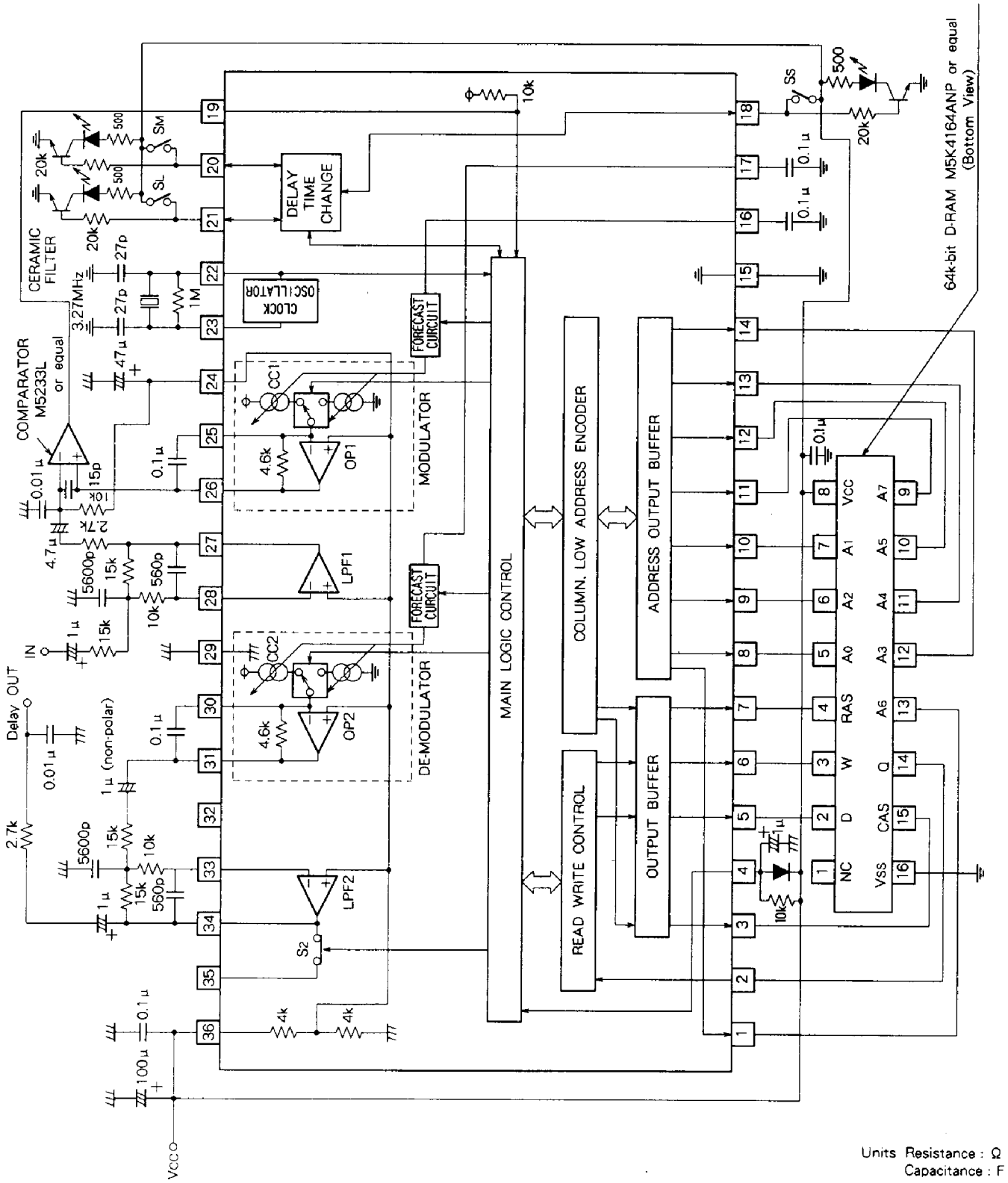
VOLTAGE GAIN VS. SUPPLY VOLTAGE



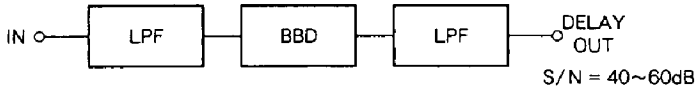
SUPPLY VOLTAGE REJECTION RATIO VS. SUPPLY VOLTAGE



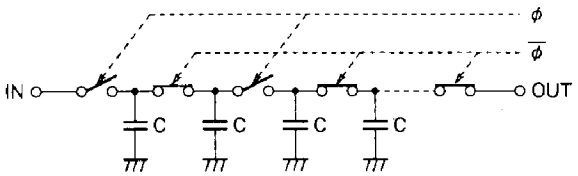
APPLICATIONS EXAMPLE



CONVENTIONAL ANALOG DELAY

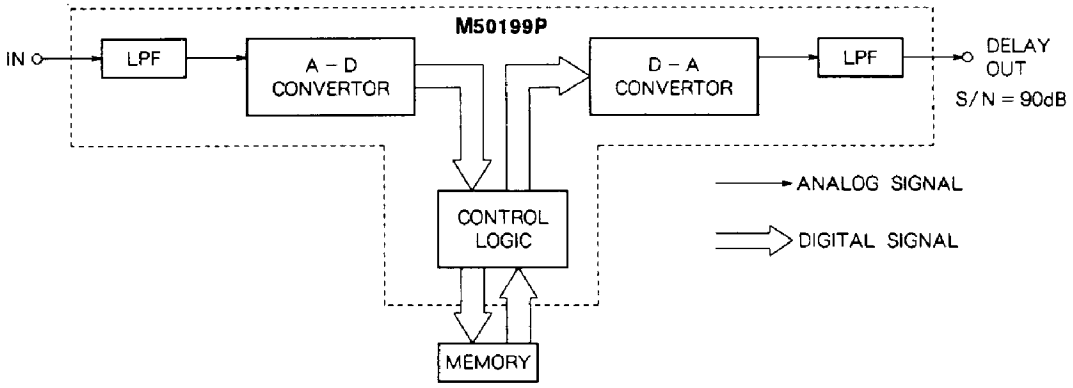


THE DELAY SYSTEM BY BBD



BBD

NEW TYPE DIGITAL DELAY



DIGITAL DELAY SYSTEM