SINGLE-CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

The MAB8021 is a single-chip 8-bit microcomputer that is fabricated using the N-MOS silicon gate process. It contains a 1K x 8 program memory, a 64 x 8 data memory, 21 I/O lines, and an 8-bit timer/event counter, in addition to on-board oscillator and clock circuits. For systems that require extra I/O capacity, the MAB8021 can be expanded using the 8243 or discrete logic.
This microcomputer is designed to be an efficient controller as well as an arithmetic computer. The MAB8021 has bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set (see Table 4) consisting mostly of single byte instructions and no instructions over two bytes in length.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 1K x 8 ROM, 64 x 8 RAM, 21 I/O lines
- Internal timer/event counter
- Clock generated with single inductor or crystal
- Single 5 V supply (range: + 4,5 V to + 6,5 V)
- 8,38 μs cycle time; all instructions 1 or 2 cycles
- Instructions: MAB8048 subset
- Zero-cross detection capability
- Easily expandable I/O

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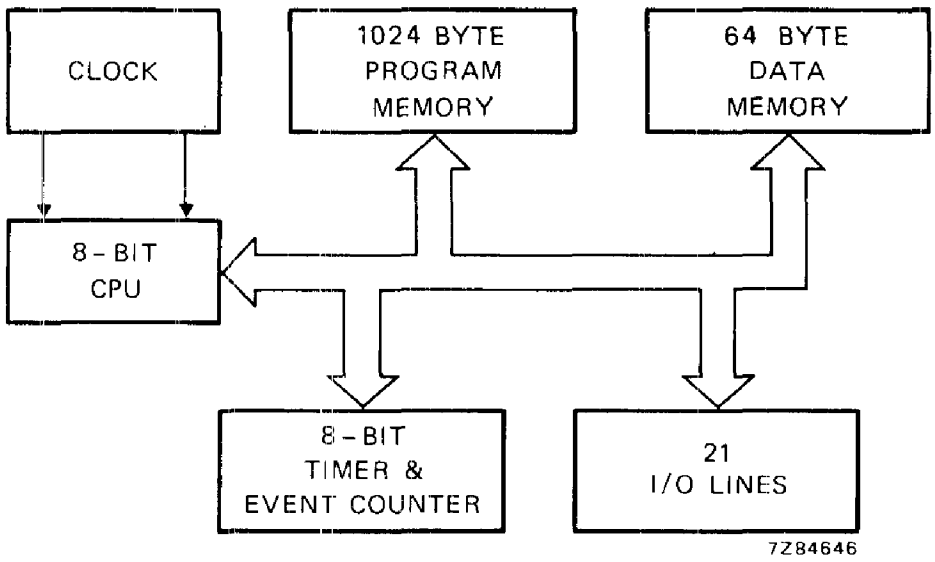


Fig. 1 Block diagram.

PACKAGE OUTLINES

MAB8021P: 28-lead DIL; plastic (SOT-117).
MAB8021D: 28-lead DIL; ceramic (SOT-135).

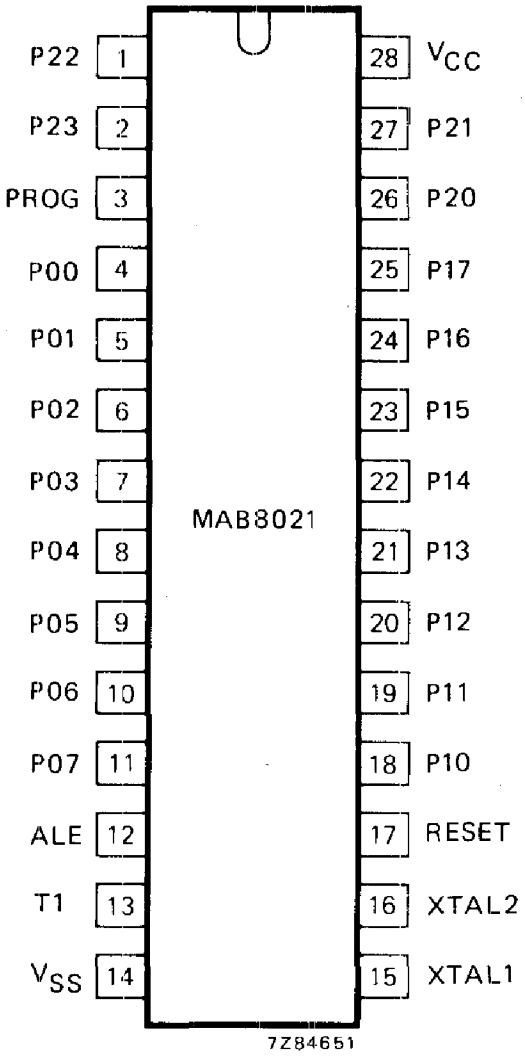


Fig. 2 Pinning diagram.

PIN DESIGNATION

designation	pin no.	function
V_{CC}	28	Power supply: + 5,5 V.
V_{SS}	14	Ground.
PROG	3	Output strobe: for 8243 I/O expander.
P00-P07	4-11	Port 0: 8-bit quasi-bidirectional port.
P10-P17	18-25	Port 1: 8-bit quasi-bidirectional port.
P20-P23	26,27,1,2	Port 2: 4-bit quasi-bidirectional port. P20-P23 also serve as a 4-bit I/O expander bus for the 8243.
T1	13	T1: input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/event counter input, using the STRT CNT instructions. Also allows zero-crossover sensing of slowly moving a.c. inputs.
RESET	17	Reset: input, used to initialize the processor by clearing status flip-flops and setting program counter to zero.
ALE	12	Address latch enable: signal occurring once every 30 input clocks, used as an output clock.
XTAL1	15	Timing control element: one side of crystal or inductor input for internal oscillator. Also the input for an external source (not TTL compatible).
XTAL2	16	Timing control element: other side.

FUNCTIONAL DESCRIPTION

The following is a functional description of the MAB8021.

Program memory

The program memory consists of a 1024 byte mask-programmed ROM. No external expansion capability is provided. The first instruction must be at location 0.

Page organization

The program memory is organized as four pages of 256 bytes each. Only the unconditional branch instruction (JMP) can cause jump over page boundaries. The CALL instruction can transfer control to a subroutine on any page. Likewise, the table data reference instruction (MOVP A,@,A) can only access data located on the same page as the instruction.

Data memory

The 64 byte dynamic RAM is organized as shown in Fig. 3. Locations (registers) 0 to 7 are directly addressable by using several instructions. All locations are indirectly addressable by using registers R0 or R1.

Address stack

Locations 8 to 23 are used as the address stack. The address stack enables the processor to keep track of the return addresses generated from CALL instructions. A 3-bit stack pointer (SP) supplies the address of the locations to be loaded with the next return address generated. The SP to this push-down stack is incremented by one after a return address is stored, and decremented by one before an address is fetched during a RET (return instruction). A total of 8 levels of nesting is possible. The SP is initialized to location 8 upon RESET.
Since each address is 10-bits long, two bytes must be used to store a single address. The SP is incremented and decremented by one, but each increment or decrement moves the address pointed to, by two. Therefore, only even numbered addresses are pointed to. If a particular application does not require 8 levels of nesting, the unused portion of the stack may be used as any other indirectly addressable scratchpad location.

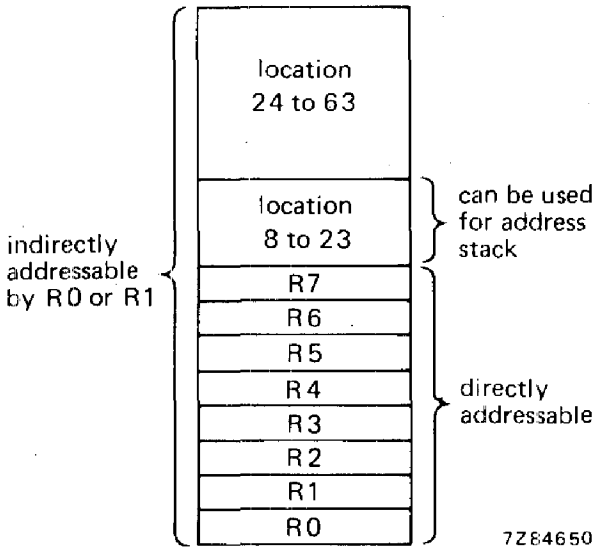


Fig. 3 Internal RAM memory map.

FUNCTIONAL DESCRIPTION (continued)

Program variable storage

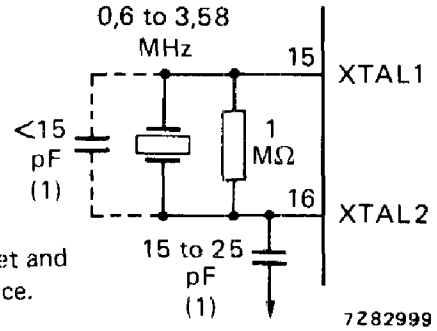
Locations 24 to 63 may be used for storage of program variables or data. In addition, any portion of the stack area (locations 8 to 23) not used for return address storage may also be used for variable storage.

Oscillator and clock

The MAB8021 contains its own internal oscillator and clock driver. The frequency is determined by a single crystal, or inductor. All internal time slots are derived from the external element, and all outputs are a function of the oscillator frequency. The particular control element is connected between pins 15 (XTAL1) and 16 (XTAL2).

An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods. Therefore, to obtain a 10 μs instruction cycle, a 3 MHz crystal should be used.

The MAB8021 utilizes dynamic RAM and certain other dynamic logic. Due to the clocking required with dynamic circuits, the oscillator frequency must be equal to or greater than 600 kHz, or improper operation may occur.



(1) Including socket and stray capacitance.

Counter/timer

The MAB8021 has an internal counter that can, under program control, count either external events (T1, pin 13) or instruction cycles. The instructions that control the counter and the functions they perform are summarized in Table 1.

The counter is an 8-bit binary up-counter. When used as a timer, the input to the counter is the overflow of a 5-bit (÷ 32) prescaler. The input of the prescaler is a signal that occurs each instruction cycle (30 clock periods).

When used as a counter, HIGH-to-LOW transitions on the T1 input are counted. The maximum frequency that can be counted is one third of the instruction cycle frequency (33,3 kHz for a 3 MHz oscillator). The positive duration of the signal must be a minimum of one tenth of the period of the instruction cycle.

When the 8-bit counter overflows, a flag is set. The flag can be tested using the JTF (jump if timer flag = 1) instruction, which resets the flag.

Table 1 Counter/timer control

function	used together counts instruction cycles		counter
	prescaler	timer	
CLEAR	STRT T	MOV T,A@(A) = 0	MOV T,A@(A) = 0
PRESET	–	MOV T,A	MOV T,A
START	STRT T	STRT T	STRT CNT
STOP	STOP TCNT	STOP TCNT or RESET	STOP TCNT or RESET
TEST	–	JTF	JTF
READ*	–	MOV A,T	MOV A,T

* READ does not disturb the counting process.

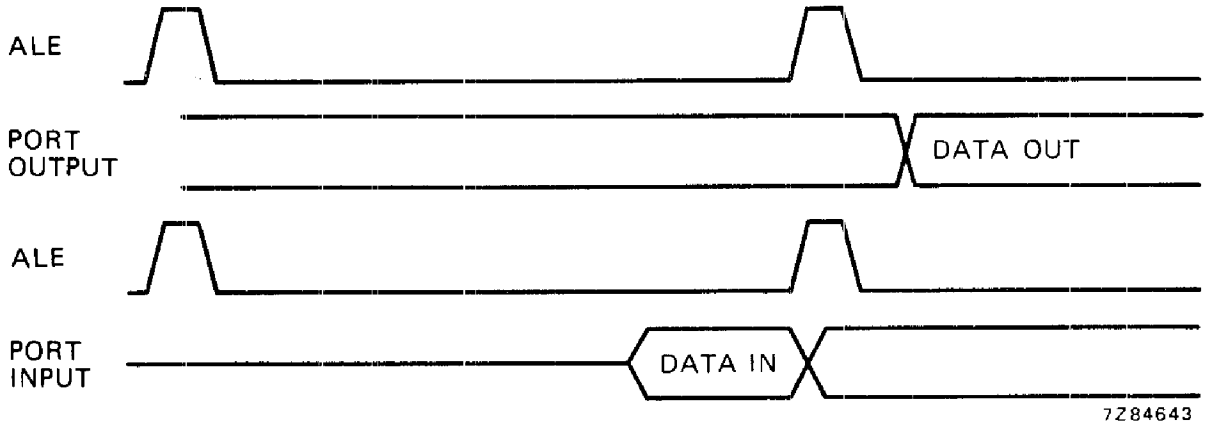


Fig. 4 Port 2 timing; normal operation.

Input/output

The 21 I/O pins are arranged as two 8-bit quasi-bidirectional ports, one 4-bit quasi-bidirectional port, and the T1 input. The 20 port pins can be individually assigned, under program control, to be either inputs or outputs (at a given time) or both (at different times).

Port operation

A simplified representation of the port circuitry is shown in Fig. 5. Output data written to a port is latched and remains unchanged until rewritten. Writing a '1' to the ports turns on the large pull-up device for less than the instruction time, which reduces the rise time of the signal. The smaller pull-up device then maintains the '1' level. The on-resistance of the small pull-up is approximately 30 kΩ. This means that, when used as an input pin, the external circuitry must sink only 0,2 mA at V_{IL}, so the MAB8021 recognizes a '0'. Thus, writing a '1' to a port-pin, it is enabled to be used either as an input pin or as a true HIGH level, latched, output pin. Writing a '0' to a port, a large pull-down device is turned on, which is capable of sinking 1,6 mA into V_{SS}. The preceding applies to ports 1 and 2.

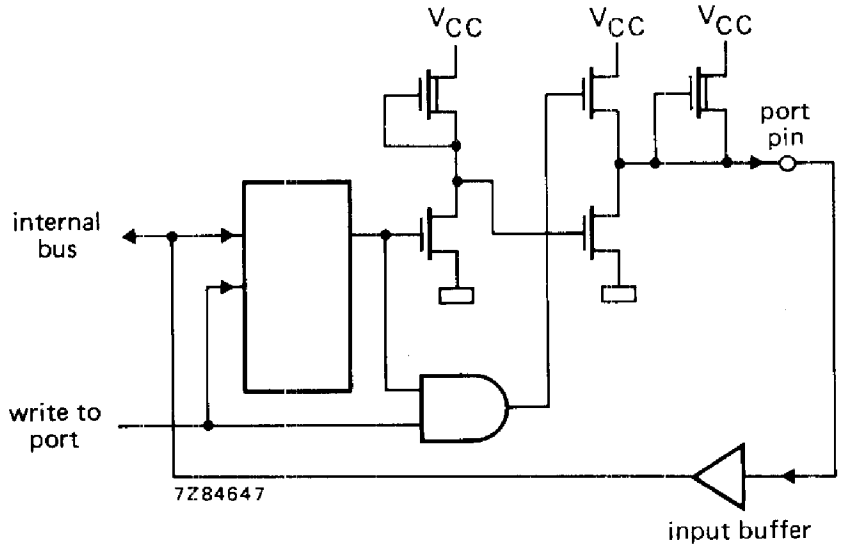


Fig. 5 Quasi-bidirectional port.

FUNCTIONAL DESCRIPTION (continued)

Port operation (continued)

Port 0 (P00 to P07) does not have the large pull-up device. In addition, by mask option, the small pull-up device (on any pin) can be deleted, thus providing a true open drain output.
The instructions ANL and ORL can be used to mask the ports, line-by-line, so that any combination of inputs and outputs can be configured on any port.

High-current outputs

Two pins (P10 and P11) are provided, which can sink larger currents (7 mA each, at V_{SS} + 2,5 V), when required. These pins may be used in parallel for 14 mA drive if the output logic states are always the same.

T1 input

The T1 input can be used for the following functions:
- event counter (external input)
- test input for branch instructions
- zero voltage cross-over detection.

The operation of T1 as an input to the event counter is described under the heading "Counter/timer".
When used as a test input, the JT1 and JNT1 instructions test for '1' and '0' levels respectively.
The T1 pin can also be used to detect the zero-crossing of slowly moving a.c. signals (50 Hz). The self-biasing circuit shown in Fig. 6 permits the T1 input to detect when the input voltage crosses zero within ± 135 mV, when the voltage is coupled through a 0,2 μF capacitor. The maximum input voltage is 3 V peak-to-peak. The zero-cross detection is especially useful in thyristor control of 50 Hz power equipment and in developing time-of-day and other timing routines. A pull-up resistor can be provided as a ROM mask option. This is useful when the input is from a switch or a standard TTL output.

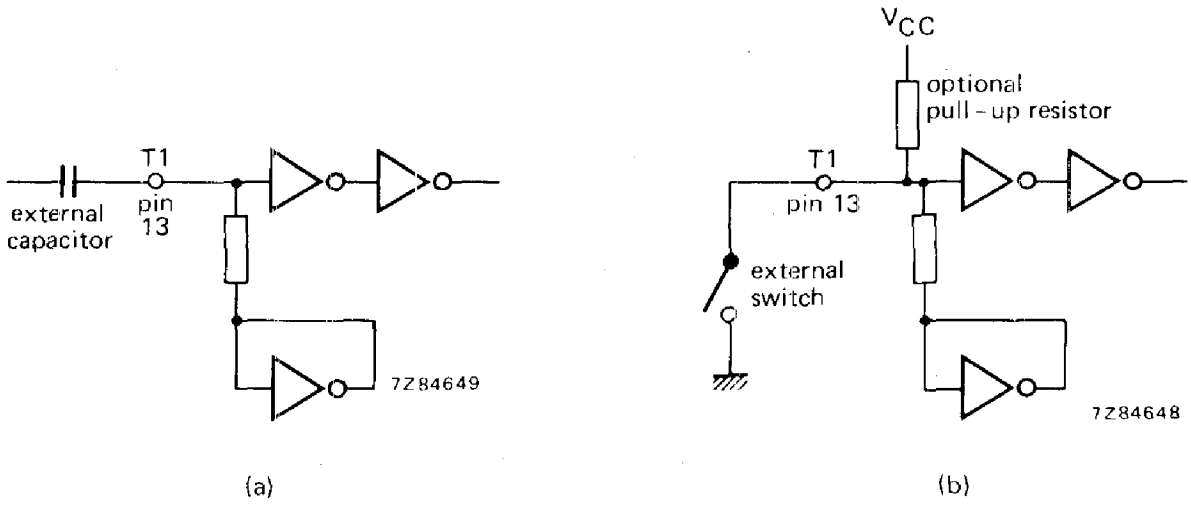


Fig. 6 T1 pin options for (a) zero-cross applications and with (b) optional pull-up resistor.

Expanded I/O

The MAB8021 can be used with the 8243 I/O expander chip, which provides additional I/O capability. The 8243 has 4 directly addressable 4-bit ports. It connects the PROG pin, which provides the clock, and pins P20 to P23, which provide address and data. These ports can be written with a MOVD P,A, ANLD P,A, and ORLD P,A for ports 4 to 7. Reading is via MOVD A,P instruction. The previous data on P20 to P23, before an output expander instruction, is lost. Therefore, when using an output expander, P20 to P23 are not useful for general input/output operation. This circuit configuration is shown in Fig. 7 and the timing diagram in Fig. 8.

The MAB8021 can also use standard low-cost TTL circuits, to expand the number of I/O lines.

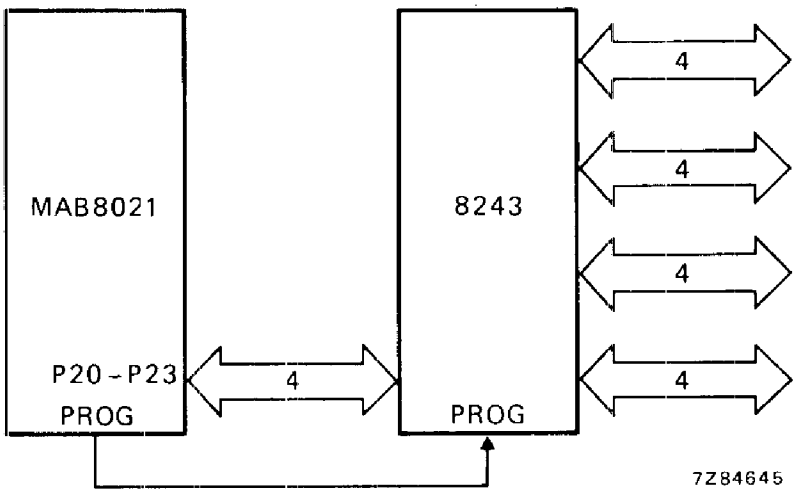


Fig. 7 Expander interface.

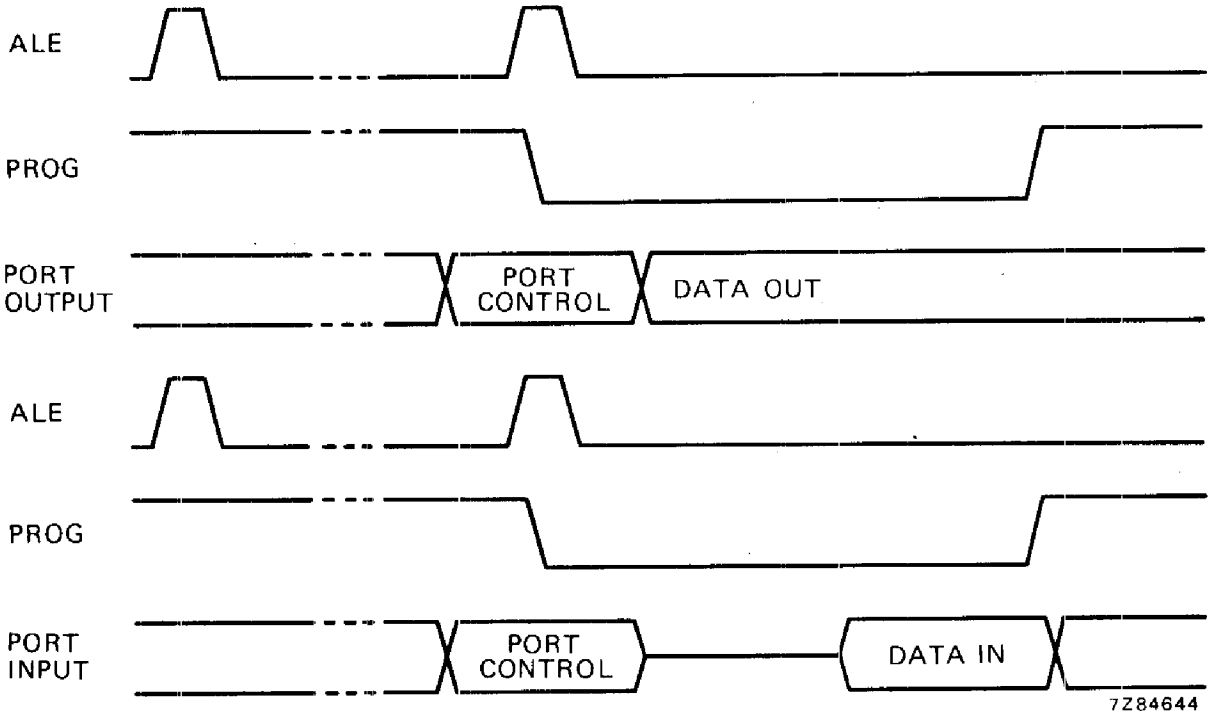


Fig. 8 Port 2 timing; expander operation.

FUNCTIONAL DESCRIPTION (continued)

Central Processing Unit

The MAB8021 has arithmetic, logical and conditional branching capabilities. The DA A, SWAP A, and XCHD instructions simplify BCD arithmetic and handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.
The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. In addition, the DJNZ instruction decrements a designated register and branches if the contents are not zero. This instruction is useful for looping control.

Testing and debug

To facilitate testing and debug, certain test modes may be activated in the MAB8021 by raising combinations of RESET, T1 and PROG to 15 V. The internal ROM is dumped out sequentially for verification. External memory operation is used for CPU check-out.

RESET	PROG	T1	case	function
5 V	X	X		power-on clear
0 V	X	X		normal operation
15 V	15 V	⎍	mode 1b	On every T1 rising edge the program counter increments, dumps internal ROM to Port 0.
0 V	15 V	X	mode 2	IC will operate from external memory (one page) via Port 0. ALE strobes address out, memory in.
15 V	X	X	mode 3	IC accepts op-codes into Port 1; allows Port 0 and 8243 testing.

X = normal mode (between 0 V and V_{CC}).

Differences between the MAB8021 and the MAB8048

Although the MAB8021 is basically an electrical and functional subset of the MAB8048, there are some differences:

1. Pin out – As the MAB8021 is a 28-lead DIL, some form of adapter must be used to interface the MAB8021 socket to ICE-49. An emulation board (EM-1) has been designed to perform this function. The EM-1 also accounts for the increased flexibility of some MAB8021 I/O lines.
2. Instruction time – The MAB8021 instruction cycle is 30 clock cycles long, the MAB8048 instruction cycle is 15 clock cycles long. Where exact timing is important, the MAB8048 bread-board part should be operated at half the MAB8021 clock rate.
3. Test 1 – To facilitate developing time-of-day routine, and for thyristor control, the T1 pin (without the pull-up resistor option) will detect zero-crossing of a capacitively coupled a.c. input.
4. Quasi-bidirectional Ports – All MAB8021 ports are quasi-bidirectional to facilitate stand-alone use. Port 0 has open drain outputs and by mask option it may or may not have pull-up resistors.
5. Oscillator – The MAB8021 has an on-chip oscillator that is optimized for the single inductor mode. External connection will differ from the MAB8048.
6. Timer/counter – 1. If prescaler overflow occurs during a 'STRT T' or 'STOP TCNT' instruction, the MAB8048 will increment the timer, while the MAB8021 will not.
   2. The MAB8021 sets the timer flag in the same cycle as the overflow. The MAB8048 waits one cycle. Therefore, the MAB8021 can do a JTF instruction one cycle earlier (prescaler = '0') than the MAB8048 (prescaler = '1').
   3. The MAB8048 doesn't increment its timer in the second cycle of a 2-cycle instruction; the MAB8021 does.
7. High-current outputs – Very high current drive is desirable for minimizing external parts required to do high-power control. P10 and P11 have been designated high drive outputs capable of sinking 7 mA at V_{SS} + 2,5 V. (For clarity, this is a 7 mA to V_{SS} with a 2,5 V drop across the buffer.) These pins may, of course, be used in parallel for 14 mA drive if the output logic states are always the same.
8. Reset – Reset has been modified on the MAB8021. On the MAB8021, RESET is active HIGH; on the MAB8048, active LOW. Also, the MAB8021 does not reset the timer flag, while the MAB8048 does.
9. Instruction set – The following instructions (see Table 2), which are found in the MAB8048, have been deleted from the MAB8021 instruction set.

Table 2 Instruction set differences

DATA MOVES		REGISTERS		BRANCH		SUBROUTINE		CONTROL		INPUT/OUTPUT	
MOV	A,PSW	DEC	R	JT0	addr	RETR		EN	I	ANL	P,#data
MOV	PSW,A	FLAGS		JNT0	addr	TIMER		DIS	I	ORL	P,#data
MOVX	A,@R			JF0	addr			SEL	RB0	INS	A,BUS*
MOVX	@R,A	CLR	F0	JF1	addr	EN	TCNTI	SEL	RB1	OUTL	BUS,A*
MOVP3	A,@A	CPL	F0	JNI	addr	DIS	TCNTI	SEL	MB0	ANL	BUS,#data
		CLR	F1	JBb	addr			SEL	MB1	ORL	BUS,#data
		CPL	F1					ENT0	CLK		

* These instructions have been replaced in the MAB8021 by INA,P0 and OUTL P0,A respectively. OUTL P0,A has op-code of MOVX @R0,A.

Table 3 Instruction set

	mnemonic		description	bytes	cycles
ACCUMULATOR	ADD	A,R	Add register to A	1	1
	ADD	A,@R	Add data memory to A	1	1
	ADD	A,#data	Add immediate to A	2	2
	ADDC	A,R	Add with carry	1	1
	ADDC	A,@R	Add with carry	1	1
	ADDC	A,#data	Add with carry	2	2
	ANL	A,R	AND register to A	1	1
	ANL	A,@R	AND data memory to A	1	1
	ANL	A,#data	AND immediate to A	2	2
	ORL	A,R	OR register to A	1	1
	ORL	A,@R	OR data memory to A	1	1
	ORL	A,#data	OR immediate to A	2	2
	XRL	A,R	Exclusive OR register to A	1	1
	XRL	A,@R	Exclusive OR data memory to A	1	1
	XRL	A,#data	Exclusive OR immediate to A	2	2
	INC	A	Increment A	1	1
	DEC	A	Decrement A	1	1
	CLR	A	Clear A	1	1
	CPL	A	Complement A	1	1
	DA	A	Decimal adjust A	1	1
	SWAP	A	Swap nibbles of A	1	1
	RL	A	Rotate A left	1	1
	RLC	A	Rotate A left through carry	1	1
	RR	A	Rotate A right	1	1
	RRC	A	Rotate A right through carry	1	1
INPUT/OUTPUT	IN	A,P	Input port to A	1	2
	OUTL	P,A	Output A to port	1	2
	MOVD	A,P	Input expander port to A	1	2
	MOVD	P,A	Output A to expander port	1	2
	ANLD	P,A	AND A to expander port	1	2
	ORLD	P,A	OR A to expander port	1	2

DEVELOPMENT SAMPLE DATA

	mnemonic		description	bytes	cycles
REG.	INC	R	Increment register	1	1
	INC	@R	Increment data memory	1	1
BRANCH	JMP	addr	Jump unconditional	2	2
	JMPP	@A	Jump in page indirect	1	2
	DJNZ	R, addr	Decrement register and jump on R not zero	2	2
	JC	addr	Jump on carry = 1	2	2
	JNC	addr	Jump on carry = 0	2	2
	JZ	addr	Jump on A zero	2	2
	JNZ	addr	Jump on A not zero	2	2
	JT1	addr	Jump on T1 = 1	2	2
	JNT1	addr	Jump on T1 = 0	2	2
	JTF	addr	Jump on timer flag	2	2
SUBR.	CALL		Jump to subroutine	2	2
	RET		Return	1	2
FLAGS	CLR	C	Clear Carry	1	1
	CPL	C	Complement Carry	1	1
DATA MOVES	MOV	A,R	Move register to A	1	1
	MOV	A,@R	Move data memory to A	1	1
	MOV	A, # data	Move immediate to A	2	2
	MOV	R,A	Move A to register	1	1
	MOV	@R,A	Move A to data memory	1	1
	MOV	R, # data	Move immediate to register	2	2
	MOV	@R, # data	Move immediate to data memory	2	2
	XCH	A,R	Exchange A and register	1	1
	XCH	A, @R	Exchange A and data memory	1	1
	XCHD	A,@R	Exchange lower nibble of A and data memory	1	1
	MOVP	A,@A	Move to A from current page	1	2
TIMER/ COUNTER	MOV	A,T	Read timer/counter	1	1
	MOV	T,A	Load timer/counter	1	1
	STRT	T	Start timer	1	1
	STRT	CNT	Start counter	1	1
	STOP	TCNT	Stop timer/counter	1	1
	NOP		No operation	1	1

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage with respect to V_{SS}	V_{CC}	−0,5 to + 7	V
Voltage on any input or output	V_I, V_O	−0,5 to + 7	V
D.C. current into any input or output	$\pm I_I$, $\pm I_O$	max. 10	mA
Total power dissipation	P_{tot}	max. 1	W
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating ambient temperature range	T_{amb}	0 to + 70	°C

D.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 0 to + 70 °C; all voltages with respect to V_{SS}; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltage	V_{CC}	4,5	5,5	6,5	V	
Supply current	I_{CC}	–	–	75	mA	
Input voltage LOW	V_{IL}	−0,5	–	0,8	V	
Input voltage HIGH all inputs except XTAL1,XTAL2,T1,RESET	V_{IH}	3,0	–	V_{CC}	V	V_{CC} = 5,5 + 1 V
Input voltage HIGH XTAL1,XTAL2,T1,RESET	V_{IH}	3,8	–	V_{CC}	V	V_{CC} = 5,5 + 1 V
Input voltage HIGH (10%) all inputs except XTAL1,XTAL2,T1,RESET	V_{IH}	2,0	–	V_{CC}	V	V_{CC} = 5,0 V ± 10%
Input voltage HIGH (10%) XTAL1,XTAL2,T1,RESET	V_{IH}	3,5	–	V_{CC}	V	V_{CC} = 5,0 V ± 10%
Output voltage LOW	V_{OL}	–	–	0,45	V	I_{OL} = 1,6 mA
Output voltage LOW P10, P11	V_{OL}	–	–	2,5	V	I_{OL} = 7 mA
Output voltage HIGH all outputs unless open drain	V_{OH}	2,4	–	–	V	$-I_{OH}$ = 50 μA
Output leakage current open drain option-port 0	$\pm I_{OL}$	–	–	10	μA	$V_{CC} \geqslant V_I \geqslant V_{SS}$ + 0,45 V

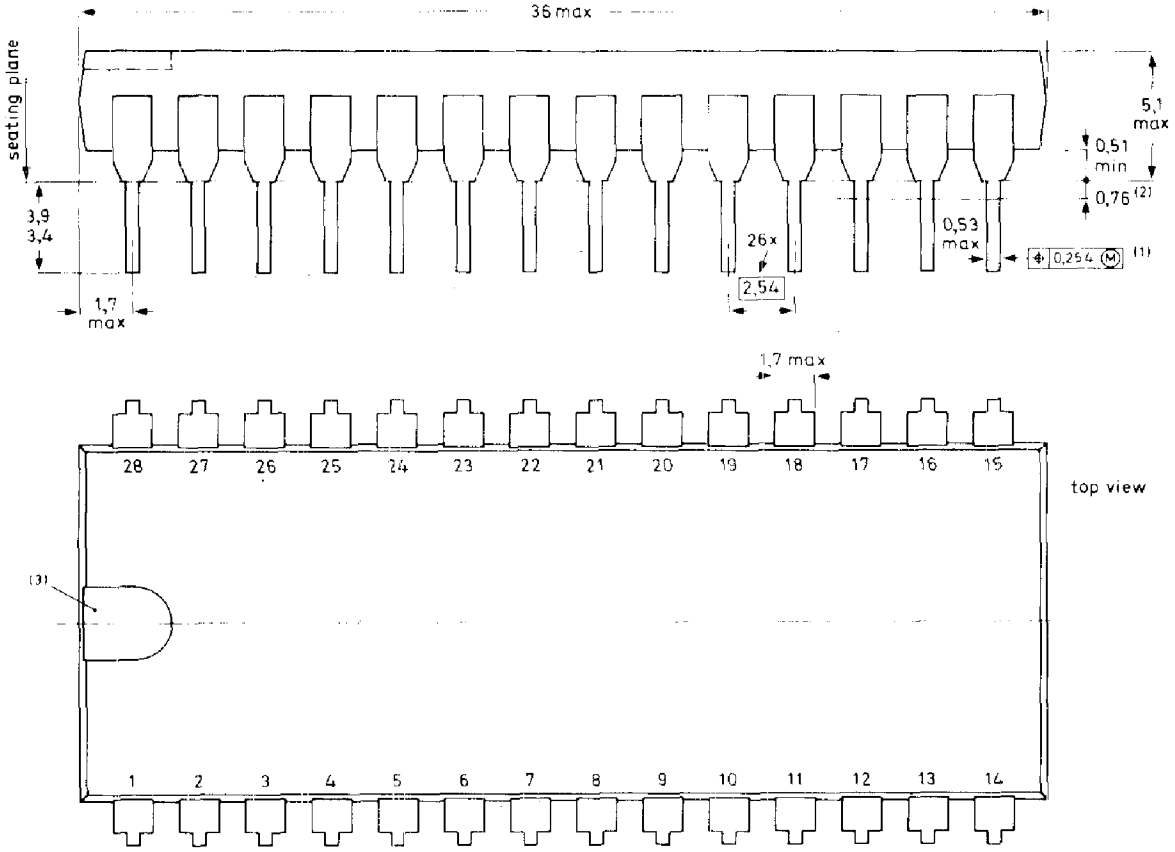
A.C. CHARACTERISTICS

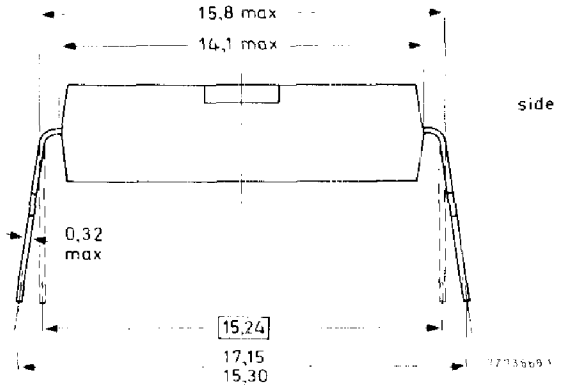
V_{SS} = 0 V; V_{CC} = 5,5 V ± 1 V; T_{amb} = 0 to + 70 °C; unless otherwise specified

	symbol	min.	typ.	max.		
Cycle time	t_{cy}	8,38	–	50,0	μs	3,58 MHz crystal = 8,38 μs
T1 zero-cross characteristics						
Zero-cross detection input (T1) voltage; peak-to-peak value	$V_{zx(p-p)}$	....	....	....	V	a.c. coupled; C = 0,2 μF
Zero-cross accuracy 50 Hz sine-wave	A_{zx}	....	....	....	mV	
Zero-cross detection input frequency (T1)	f_{T1}	....	....	....	kHz	

DEVELOPMENT SAMPLE DATA

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

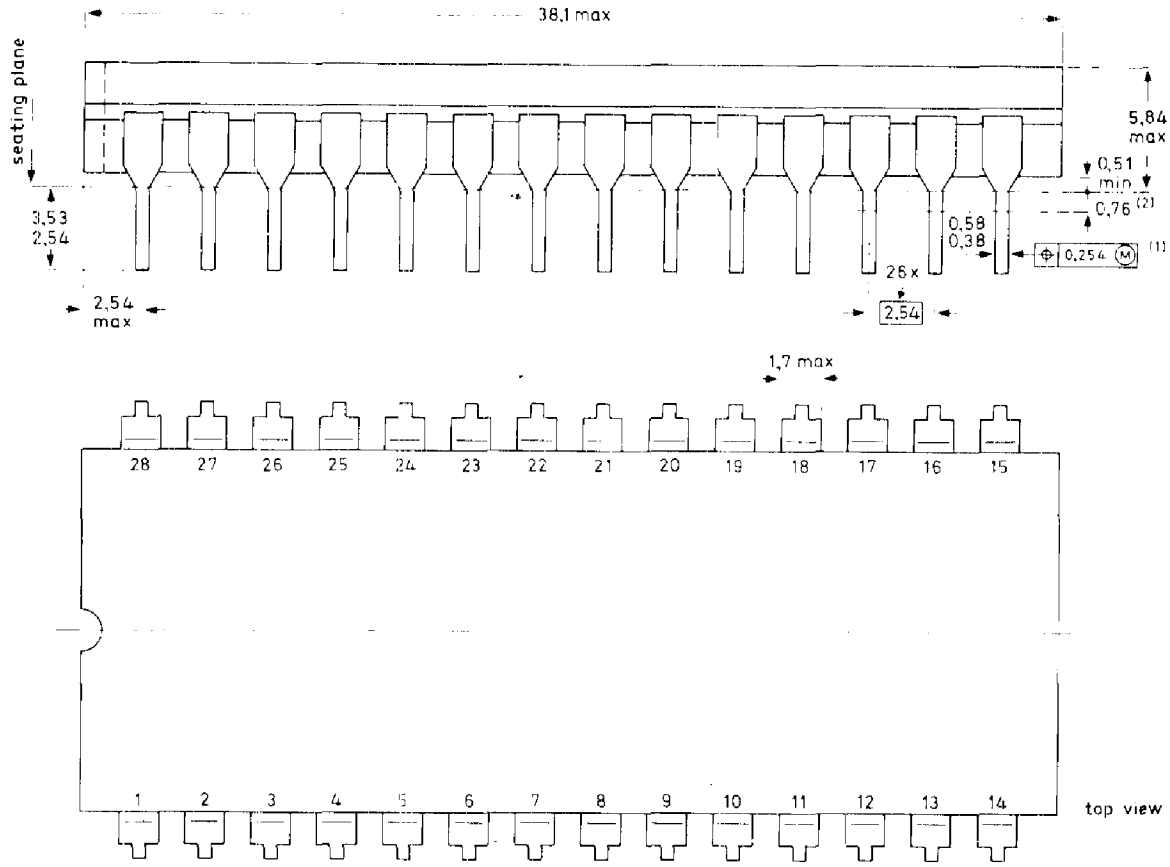
2. By dip or wave

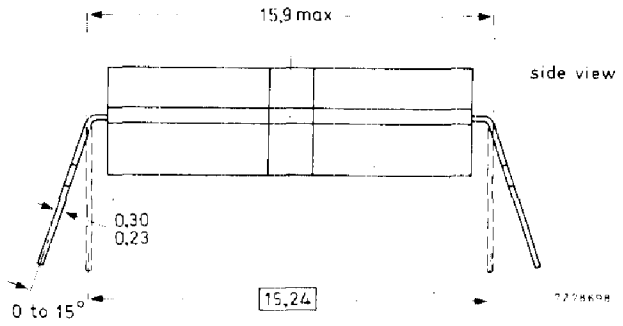
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

28-LEAD DUAL IN-LINE; CERAMIC (SOT-135)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.