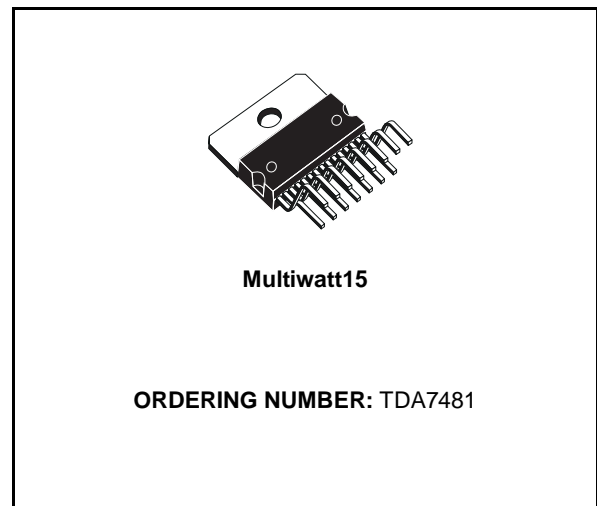


## 18W MONO CLASS-D AMPLIFIER

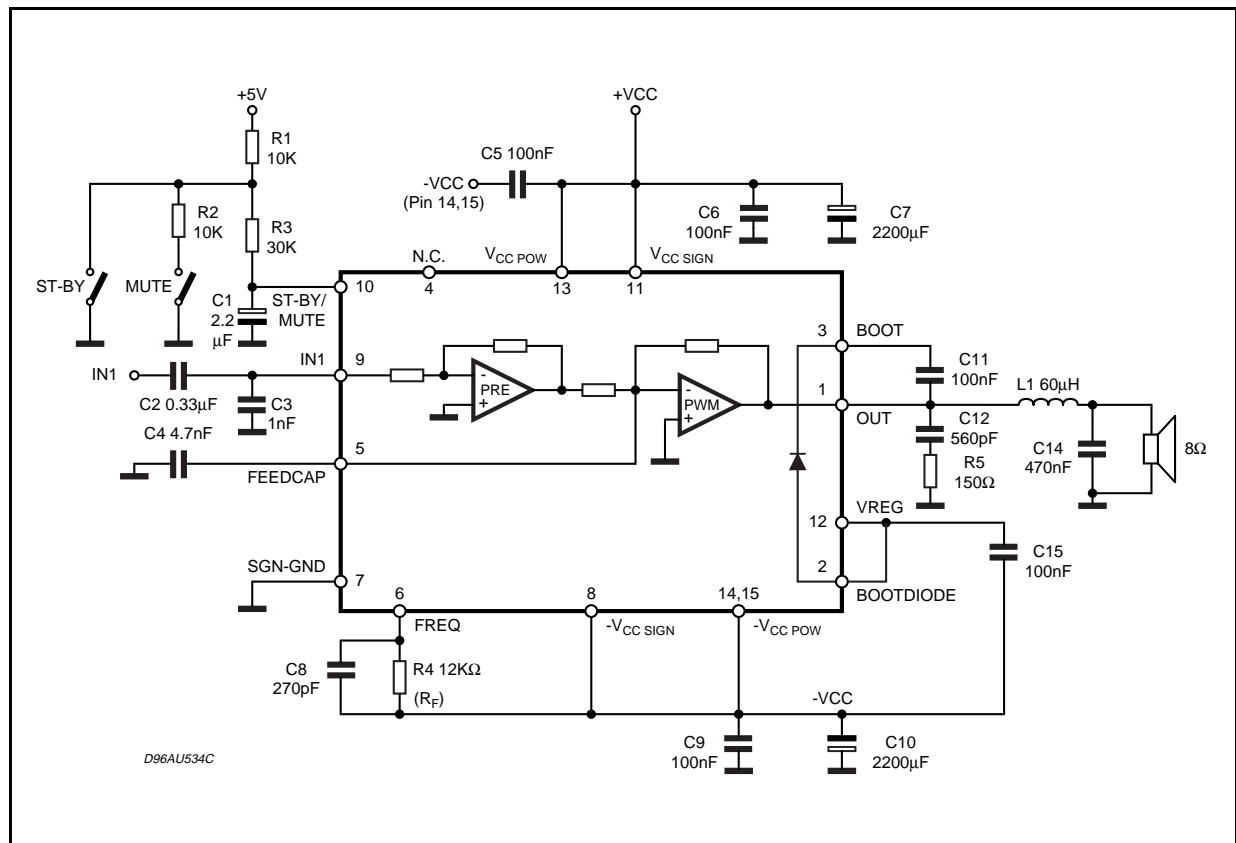
- 18W OUTPUT POWER:  
 $R_L = 8\Omega/4\Omega$ ; THD = 10%
- HIGH EFFICIENCY
- WIDE SUPPLY VOLTAGE RANGE (UP TO  $\pm 25V$ )
- SPLIT SUPPLY
- OVERVOLTAGE PROTECTION
- ST-BY AND MUTE FEATURES
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

### DESCRIPTION

The TDA7481 is an audio class-D amplifier assembled in Multiwatt15 package specially designed for high efficiency applications mainly for TV and Home Stereo sets.



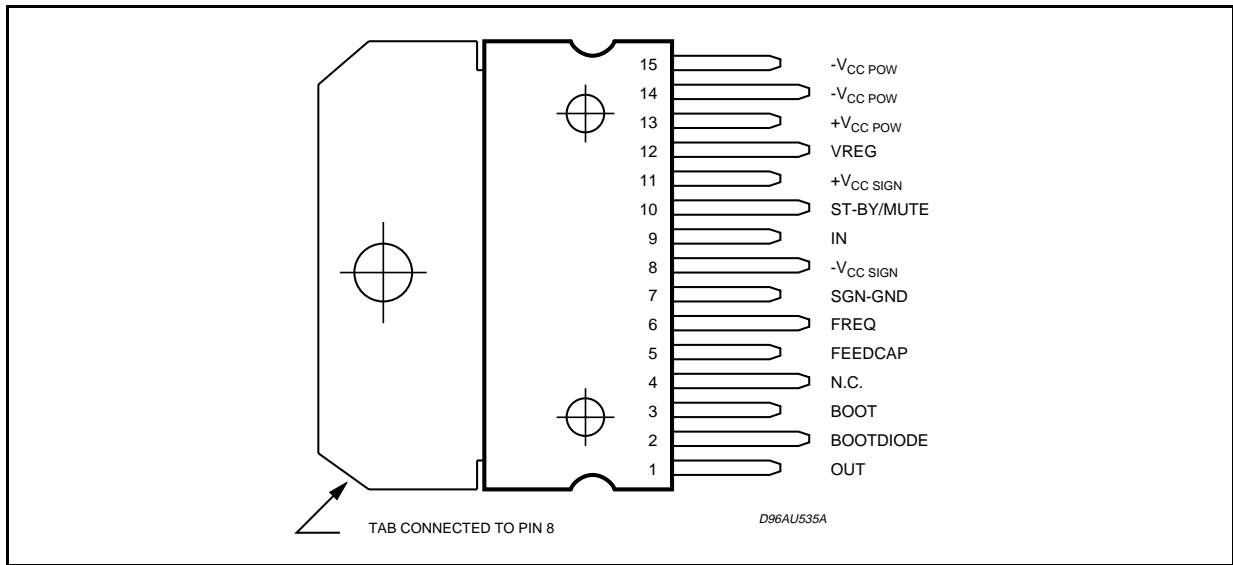
**Figure 1:** Test and Application Circuit.



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	$\pm 25$	V
$P_{tot}$	Power Dissipation $T_{case} = 70^{\circ}C$	35	W
$T_{stg}, T_j$	Storage and Junction Temperature	-40 to 150	$^{\circ}C$
$V_{FREQ}$	Maximum Voltage Across RF (pin 6)	8	V
$T_{op}$	Operating Temperature Range	0 to 70	$^{\circ}C$
ESD	Max ESD On Pins	$\pm 1.2$	KV

**PIN CONNECTION (Top view)**



**THERMAL DATA**

Symbol	Parameter	Typ.	Max.	Unit
$R_{th\ j-case}$	Thermal Resistance Junction-case	1.8	2.5	$^{\circ}C/W$

**PIN FUNCTIONS**

N.	Name	Function
1	OUT	PWM OUTPUT
2	BOOTDIODE	BOOTSTRAP DIODE ANODE
3	BOOT	BOOTSTRAP
4	NC	NOT CONNECTED
5	FEEDCAP	FEEDBACK INTEGRATING CAPACITOR
6	FREQ	SETTING FREQUENCY RESISTOR
7	SGN-GND	SIGNAL GROUND
8	$-V_{CC\ SIGN}$	SIGNAL NEGATIVE SUPPLY
9	IN	INPUT
10	ST-BY/MUTE	CONTROL STATE PIN
11	$+V_{CC\ SIGN}$	POSITIVE SIGNAL SUPPLY
12	VREG	INTERNAL VOLTAGE REGULATOR
13	$+V_{CC\ POW}$	POSITIVE POWER SUPPLY
14	$-V_{CC\ POW}$	NEGATIVE POWER SUPPLY (to be connected to pin 13 via CS)
15	$-V_{CC\ POW}$	NEGATIVE POWER SUPPLY (to be connected to pin 13 via CS)

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit,  $V_{CC} = \pm 18V$ ;  $R_L = 8\Omega$ ;  $R_S = 50\Omega$ ;  $R_F = 12K\Omega$ ; Demod.. filter  $L = 60\mu H$ ,  $C = 470nF$ ;  $f = 1KHz$ ;  $T_{amb} = 25^\circ C$  unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_S$	Supply Range		$\pm 10$		$\pm 25$	V
$I_q$	Total Quiescent Current	$R_L = \infty$ , no LC filter		35	55	mA
$V_{OS}$	Output Offset Voltage	PLAY condition	-70	-30	10	mV
$P_O$	Output Power	THD = 10% THD = 1%	15 10	18 13		W W
$P_O$	Output Power	$V_{CC} = \pm 15V$ ; $R_L = 4\Omega$ THD = 10% THD = 1% (*)		18 13		W W
$P_D$	Maximum Dissipated Power	$V_{CC} = \pm 18V$ ; $R_L = 8\Omega$ ; $R_f = 12K\Omega$ $P_O = 18W$ THD 10%		3.5		W
$\eta$	Efficiency $\equiv \frac{P_O}{P_O + P_D} \equiv \frac{P_O}{P_i}$ (**)	$V_{CC} = \pm 18V$ ; $R_L = 8\Omega$ ; $R_f = 12K\Omega$ $P_O = 18W$ THD 10%		85		%
THD	Total Harmonic Distortion	$R_L = 8\Omega$ ; $P_O = 1W$		0.1		%
$I_{max}$	Overcurrent Protection Threshold	$R_L = 0$	3.5	5		A
$T_j$	Thermal Shut-down Junction Temperature			150		$^\circ C$
$G_V$	Closed Loop Gain		29	30	31	dB
$e_N$	Total Input Noise	A Curve $f = 20Hz$ to $22KHz$		7 12		$\mu V$ $\mu V$
$V_{CCTOT MAX}$	Maximum Total $V_{CC}$ Protection		50			V
$R_i$	Input Resistance		20	30		$k\Omega$
SVR	Supply Voltage Rejection	$f = 100Hz$ ; $V_r = 0.5$	46	60		dB
$T_r, T_f$	Rising and Falling Time			50		ns
$R_{DSON}$	Power Transistor on Resistance			0.4		$\Omega$
$F_{SW-OP}$	Switching Frequency Operative Range		100		200	KHz
$F_{SW}$	Switching Frequency		100	120	140	KHz
$B_F$	Zero Signal Frequency Constant (***)			$1.4 \times 10^9$		Hz $\Omega$
$R_F$	Frequency Controller Resistor Range (****)		7	12	14	$K\Omega$
<b>MUTE &amp; STAND-BY FUNCTIONS</b>						
$V_{ST-BY}$	Stand-by range				0.8	V
$V_{MUTE}$	Mute Range		1.8		2.5	V
$V_{PLAY}$	Play Range (1)		4			V
$A_{MUTE}$	Mute Attenuation		60	80		dB
$I_{qST-BY}$	Quiescent Current @ Stand-by			3	5	mA

\*: The output LC filter must be changed to:  $L = 30\mu H$ ;  $C = 1\mu F$

\*\* $P_O$  = measured across the load using the following inductor:  
COIL 58120 MPPA2 (magnetics)      TURNS: 28  $\varnothing$  1mm

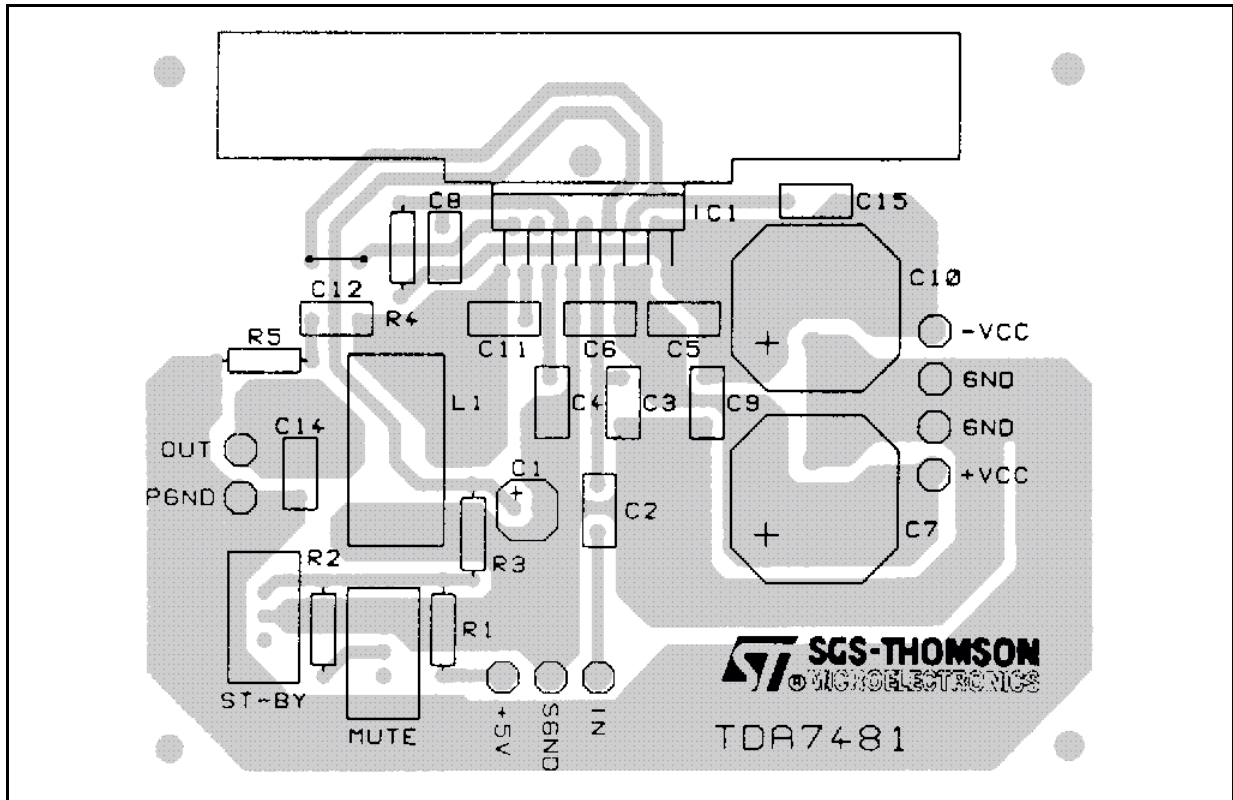
\*\*\*: The zero-signal switching frequency can be obtained using the following expression:  $F_{SW} = B_F/R_F$

\*\*\*\*: The maximum value of  $R_F$  is related to the maximum possible value for the voltage drop on  $R_F$  itself

(1) for  $V_{IO} > 5.2V$ , an input impedance of  $10K\Omega$  is to be considered

# TDA7481

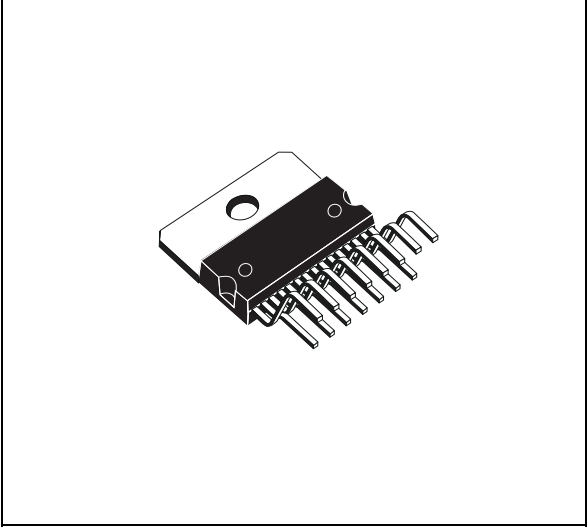
Figure 2: Recommended P.C. Board and Component Layout of the Circuit of Figure 1 (1.25:1 scale)



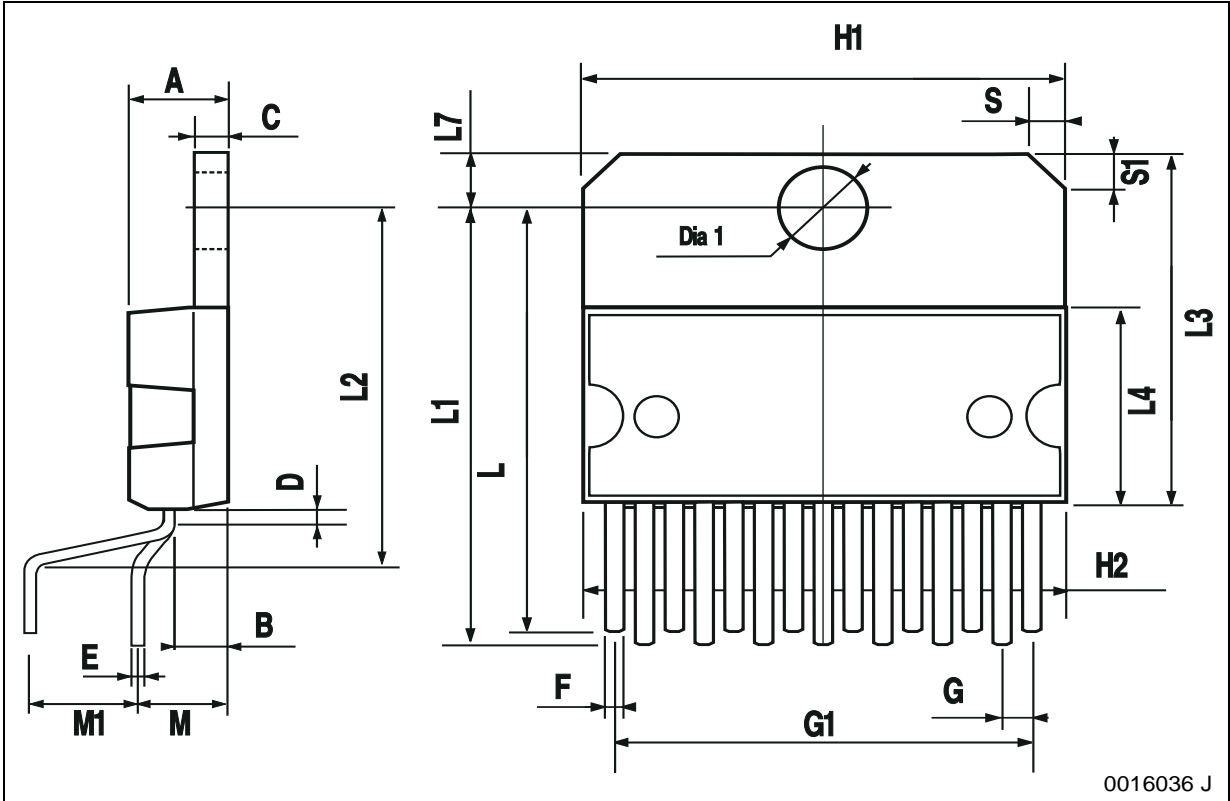
Note: Capacitor C5 must be as close as possible to device's pins 16 and 17

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A5						0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.87	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.73	5.08	5.43	0.186	0.200	0.214
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

**OUTLINE AND MECHANICAL DATA**



**Multiwatt15 (Vertical)**



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