

## CMOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

■ CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor ( $R_X$ ) and an external capacitor ( $C_X$ ) control the timing for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of  $R_X$  and  $C_X$ .

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to  $V_{SS}$ . An unused -TR input should be tied to  $V_{DD}$ . A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to  $V_{DD}$ . However, if an entire section of the CD4098B is not used, its RESET should be tied to  $V_{SS}$ . See Table I.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode,  $\bar{Q}$  is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used.

The time period (T) for this multivibrator can be approximated by:  $T_X = \frac{1}{2} R_X C_X$  for  $C_X \geq 0.01 \mu\text{F}$ . Time periods as a function of  $R_X$  for values of  $C_X$  and  $V_{DD}$  are given in Fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and  $R_X C_X$ .

The minimum value of external resistance,  $R_X$ , is 5 k $\Omega$ . The maximum value of external capacitance,  $C_X$ , is 100  $\mu\text{F}$ . Fig. 9 shows time periods as a function of  $C_X$  for values of  $R_X$  and  $V_{DD}$ .

The output pulse width has variations of  $\pm 2.5\%$  typically, over the temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for  $C_X = 1000 \text{ pF}$  and  $R_X = 100 \text{ k}\Omega$ .

For power supply variations of  $\pm 5\%$ , the output pulse width has variations of  $\pm 0.5\%$  typically, for  $V_{DD} = 10 \text{ V}$  and  $15 \text{ V}$  and  $\pm 1\%$  typically, for  $V_{DD} = 5 \text{ V}$  at  $C_X = 1000 \text{ pF}$  and  $R_X = 5 \text{ k}\Omega$ .

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and MT suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

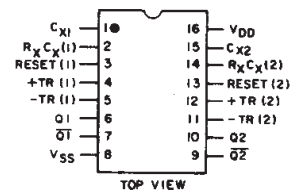
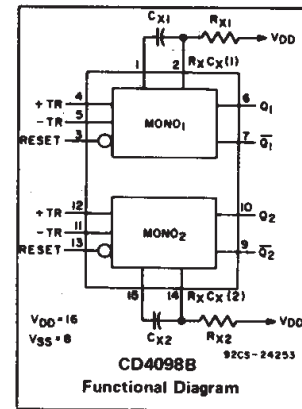
The CD4098B is similar to type MC14528.

### Features:

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of  $R_X$ ,  $C_X$
- Triggering from leading or trailing edge
- Q and  $\bar{Q}$  buffered outputs available
- Separate resets
- Wide range of output-pulse widths
- 100% tested for maximum quiescent current at 20 V
- Maximum input current of 1  $\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and  $25^\circ\text{C}$
- Noise margin (full package-temperature range):
  - 1 V at  $V_{DD} = 5 \text{ V}$
  - 2 V at  $V_{DD} = 10 \text{ V}$
  - 2.5 V at  $V_{DD} = 15 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

### Applications:

- Pulse delay and timing
- Pulse shaping
- Astable multivibrator



TERMINALS 1, 8, 15 ARE  
ELECTRICALLY CONNECTED  
INTERNALLY

92CS-24848R1

### TERMINAL ASSIGNMENT

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	Voltages referenced to $V_{SS}$ Terminal)		-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS			-0.5V to $V_{DD} + 0.5\text{V}$
DC INPUT CURRENT, ANY ONE INPUT			$\pm 10 \text{ mA}$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):			
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$			500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$			Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR			
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$			100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )			$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )			$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):			
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79 \text{ mm}$ ) from case for 10s max			$+265^\circ\text{C}$

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	$V_{DD}$ V	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ )	-	3	18	V
Trigger Pulse Width $t_W(\text{TR})$	5 10 15	140 60 40	- - -	ns
Reset Pulse Width $t_W(\text{R})$ (This is a function of $C_X$ )	-	See Dynamic Char. Chart and Fig. 10		-
Trigger Rise or Fall Time $t_r(\text{TR}), t_f(\text{TR})$	5-15	-	100	$\mu\text{s}$

# CD4098B Types

TABLE I  
CD4098B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V <sub>DD</sub> TO TERM. NO.		V <sub>SS</sub> TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T<sub>X</sub>) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T<sub>X</sub> REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

The minimum time between retriggering edges (or trigger and retrigger edges) is 40 per cent of (T<sub>X</sub>).

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

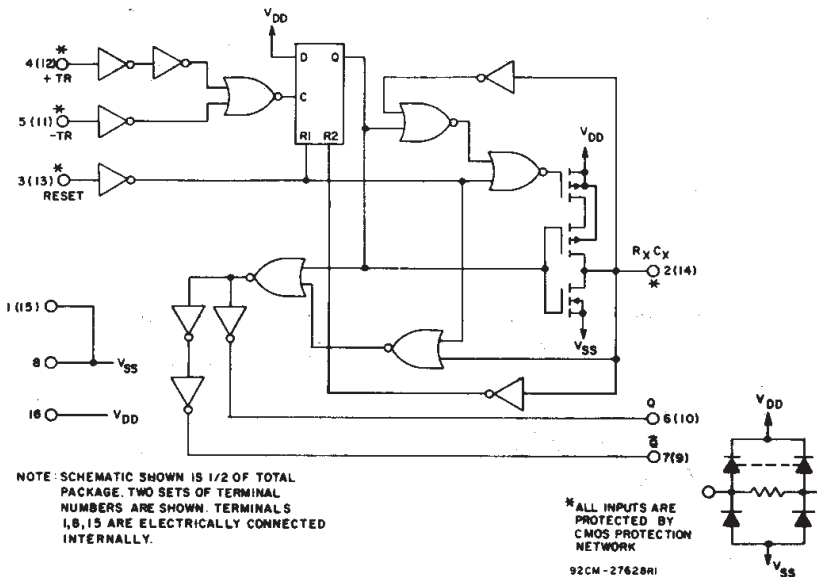
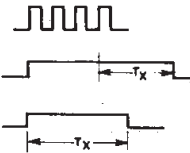


Fig. 4 - CD4098B logic diagram.

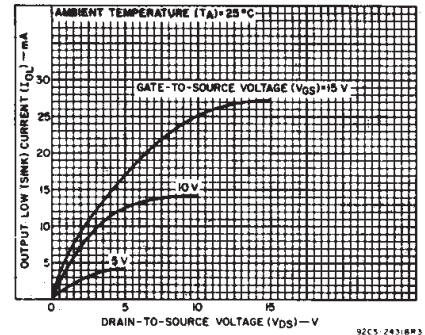


Fig. 1 - Typical output low (sink) current characteristics.

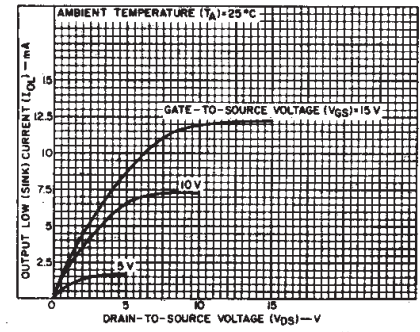


Fig. 2 - Minimum output low (sink) current characteristics.

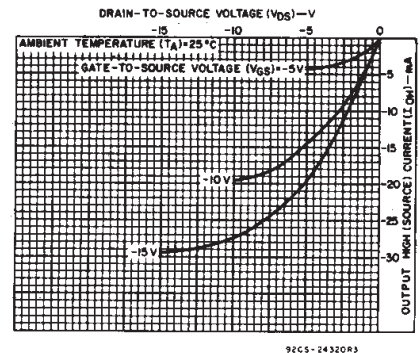


Fig. 3 - Typical output high (source) current characteristics.

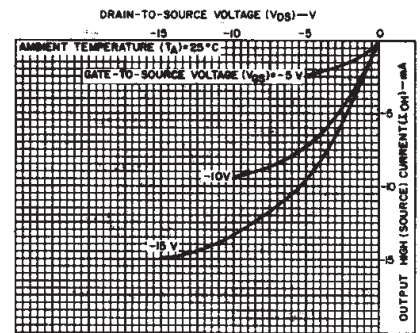


Fig. 5 - Minimum output high (source) current characteristics.

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## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current	—	0.5	5	1	1	30	30	—	0.02	1	μA
I <sub>DD</sub> Max.	—	0.10	10	2	2	60	60	—	0.02	2	
	—	0.15	15	4	4	120	120	—	0.02	4	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0.5	5				0.05			0.05	V
	—	0.10	10				0.05			0.05	
	—	0.15	15				0.05			0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0.5	5				4.95			5	V
	—	0.10	10				9.95			10	
	—	0.15	15				14.95			15	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5				1.5			1.5	V
	1.9	—	10				3			3	
	1.5, 13.5	—	15				4			4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5				3.5			3.5	V
	1.9	—	10				7			7	
	1.5, 13.5	—	15				11			11	
Input Current, I <sub>IN</sub> Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

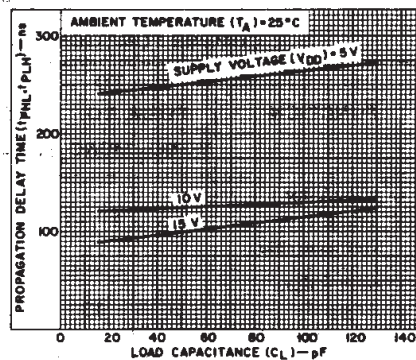


Fig. 6 - Typical propagation delay time vs. load capacitance, trigger into Q out. (All values of C<sub>X</sub> and R<sub>X</sub>.)

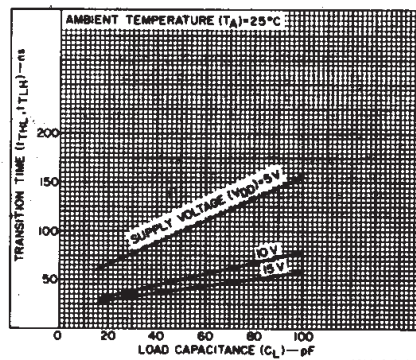


Fig. 7 - Transition time vs. load capacitance for R<sub>X</sub> = 5 kΩ-10000 kΩ and C<sub>X</sub> = 15 pF-10000 pF.

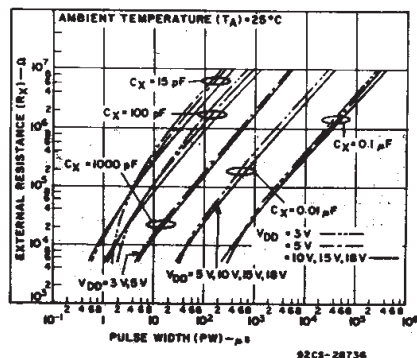


Fig. 8 - Typical external resistance vs. pulse width.

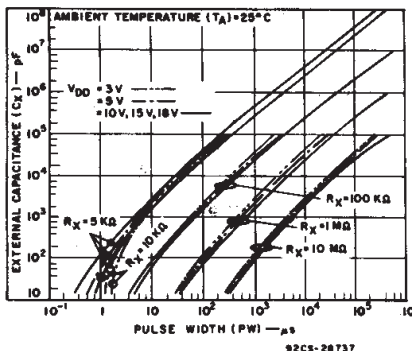


Fig. 9 - Typical external capacitance vs. pulse width.

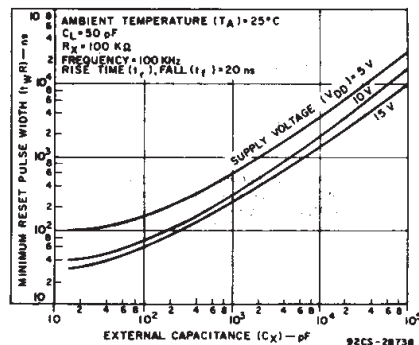


Fig. 10 - Typical minimum reset pulse width vs. external capacitance.

# CD4098B Types

## DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS		
	$R_X$ (k $\Omega$ )	$C_X$ (pF)	$V_{DD}$ (V)	Typ.	Max.			
Trigger Propagation Delay Time +TR, -TR to Q, $\bar{Q}$ $t_{PHL}$ , $t_{PLH}$	5 to 10,000	$\geq 15$	5 10 15	250 125 100	500 250 200	ns		
Minimum Trigger Pulse Width, $t_{WH}$ , $t_{WL}$	5 to 10,000	$\geq 15$	5 10 15	70 30 20	140 60 40	ns		
Transition Time, $t_{TLH}$	5 to 10,000	$\geq 15$	5 10 15	100 50 40	200 100 80	ns		
$t_{THL}$	5 to 10,000	15 to 10,000	5 10 15	100 50 40	200 100 80			
	5 to 10,000	0.01 $\mu\text{F}$ to 0.1 $\mu\text{F}$	5 10 15	150 75 65	300 150 130			
	5 to 10,000	0.1 $\mu\text{F}$ to 1 $\mu\text{F}$	5 10 15	250 150 80	500 300 160			
Reset Propagation Delay Time, $T_{PHL}$ , $T_{PLH}$	5 to 10,000	$\geq 15$	5 10 15	225 125 75	450 250 150	ns		
Minimum Reset Pulse Width, $t_{WR}$	100	15	5	100	200	ns		
			10	40	80			
			15	30	60			
		1000	5	600	1200	$\mu\text{s}$		
10	300	600						
15	250	500						
Trigger Rise or Fall Time $t_r$ (TR), $t_f$ (TR)	-	-	5 to 15	-	100	$\mu\text{s}$		
			10	10,000	5	5	10	%
					10	7.5	15	
Pulse Width Match Between Circuits in Same Package	10	10,000	5 10 15	5 7.5 7.5	10 15 15			
Input Capacitance, $C_{iN}$	Any Input			5	7.5	pF		

## TEST CIRCUITS

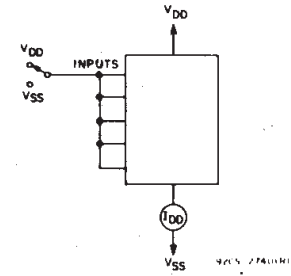


Fig. 12 - Quiescent-device-current test circuits.

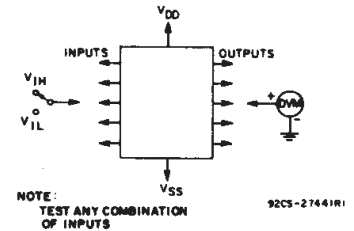


Fig. 13 - Input-voltage test circuit.

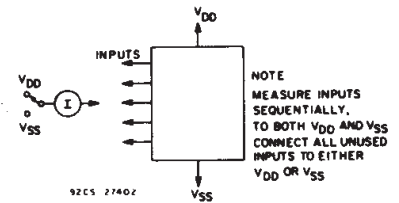


Fig. 14 - Input leakage current test circuit.

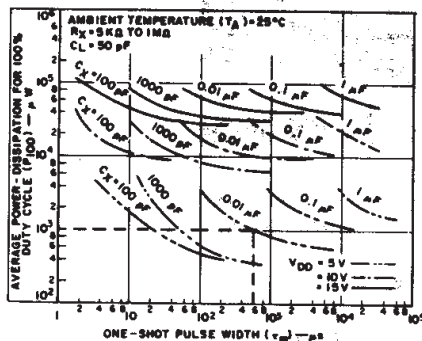
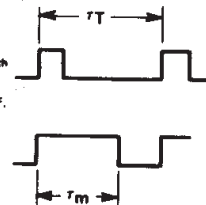


Fig. 11 - Average power dissipation vs. one-shot pulse width.

To calculate average power dissipation (P) for less than 100% duty cycle:  
 $P_{100}$  = average power for 100% duty cycle  
 $P = \left(\frac{t_m}{T_T}\right) P_{100}$  where  $t_m$  = one-shot pulse width  
 $T_T$  = trigger pulse period  
 e.g. For  $t_m = 800\ \mu\text{s}$ ,  $T_T = 1000\ \mu\text{s}$ ,  $C_X = 0.01\ \mu\text{F}$ ,  
 $V_{DD} = 5\text{ V}$   
 $P = \left(\frac{800}{1000}\right) 10^3\ \mu\text{W} = 800\ \mu\text{W}$  (see dotted line on graph)



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## APPLICATIONS

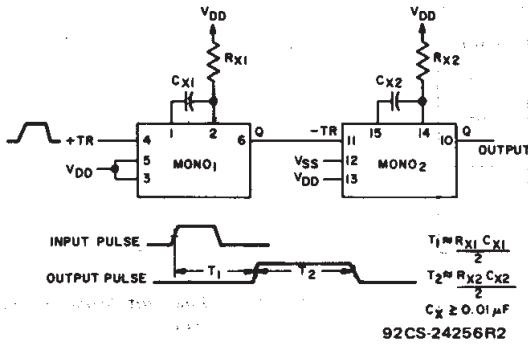


Fig. 15 - Pulse delay.

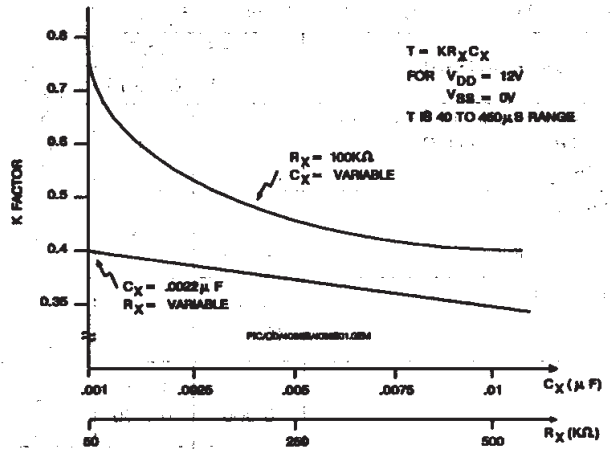


Fig. 17 - K-Factor for  $V_{DD} = 12V$ .

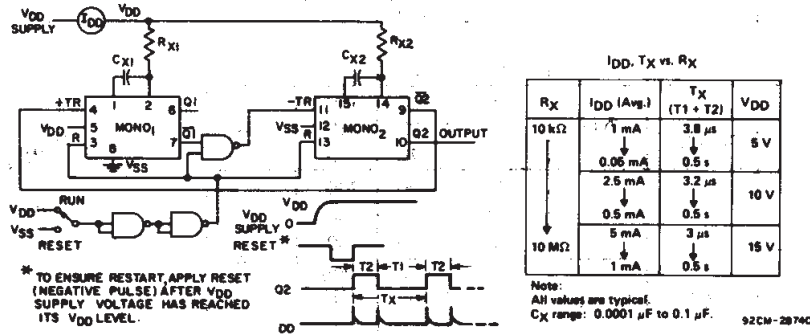
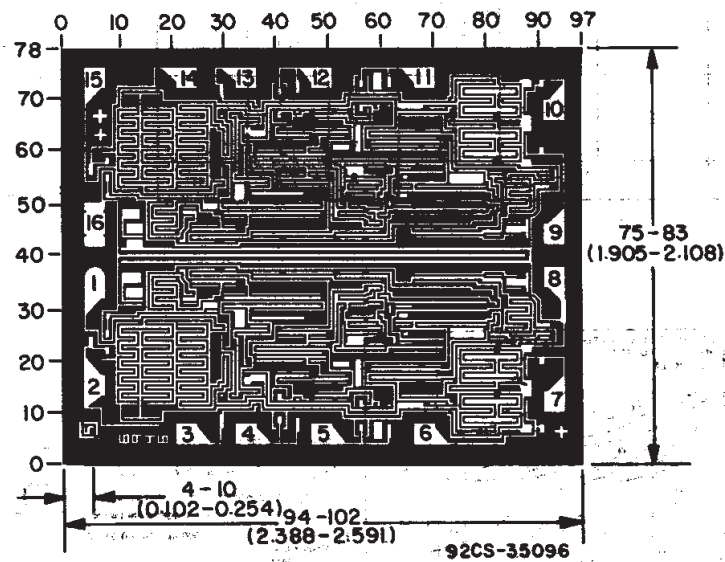


Fig. 16 - Astable multivibrator with restart after reset capability.



### Dimensions and Pad Layout for CD4098BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD4098BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4098BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4098BF	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD4098BF3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD4098BFB	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD4098BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4098BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/17504BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

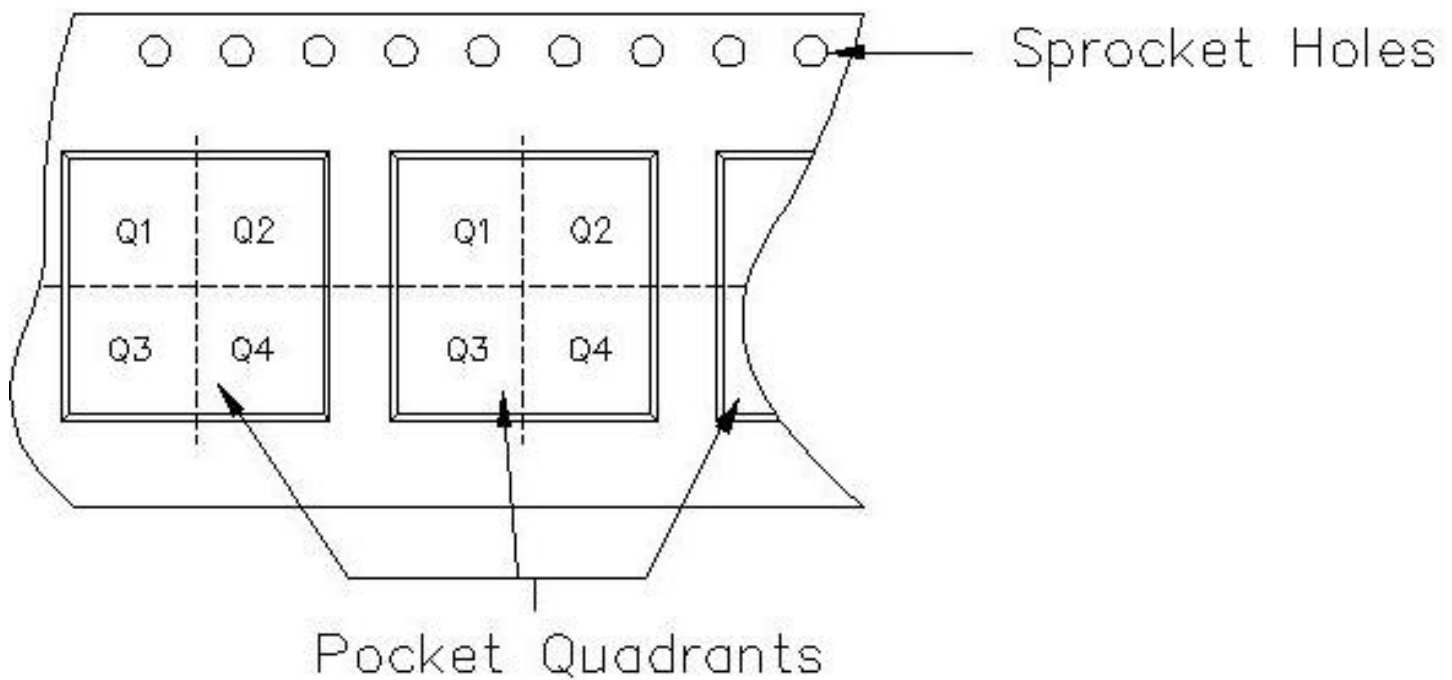
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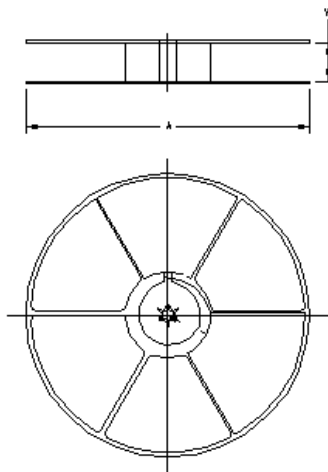
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



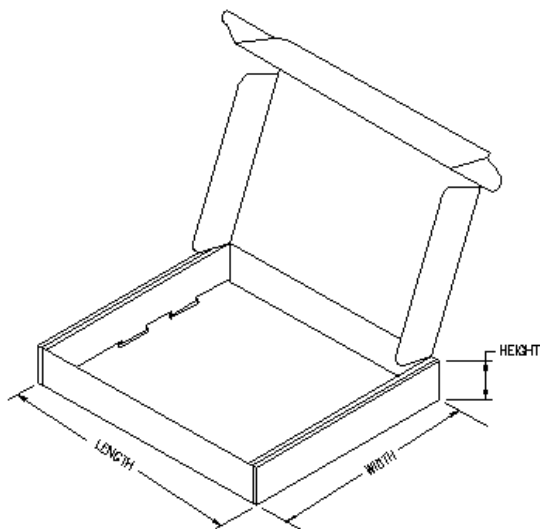
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4098BM96	D	16	FMX	0	16	6.5	10.3	12.1	2	16	Q1
CD4098BPWR	PW	16	MLA	330	12	7.0	5.6	1.6	8	12	Q1



**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD4098BM96	D	16	FMX	333.2	333.2	28.58
CD4098BPWR	PW	16	MLA	338.1	340.5	20.64



J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

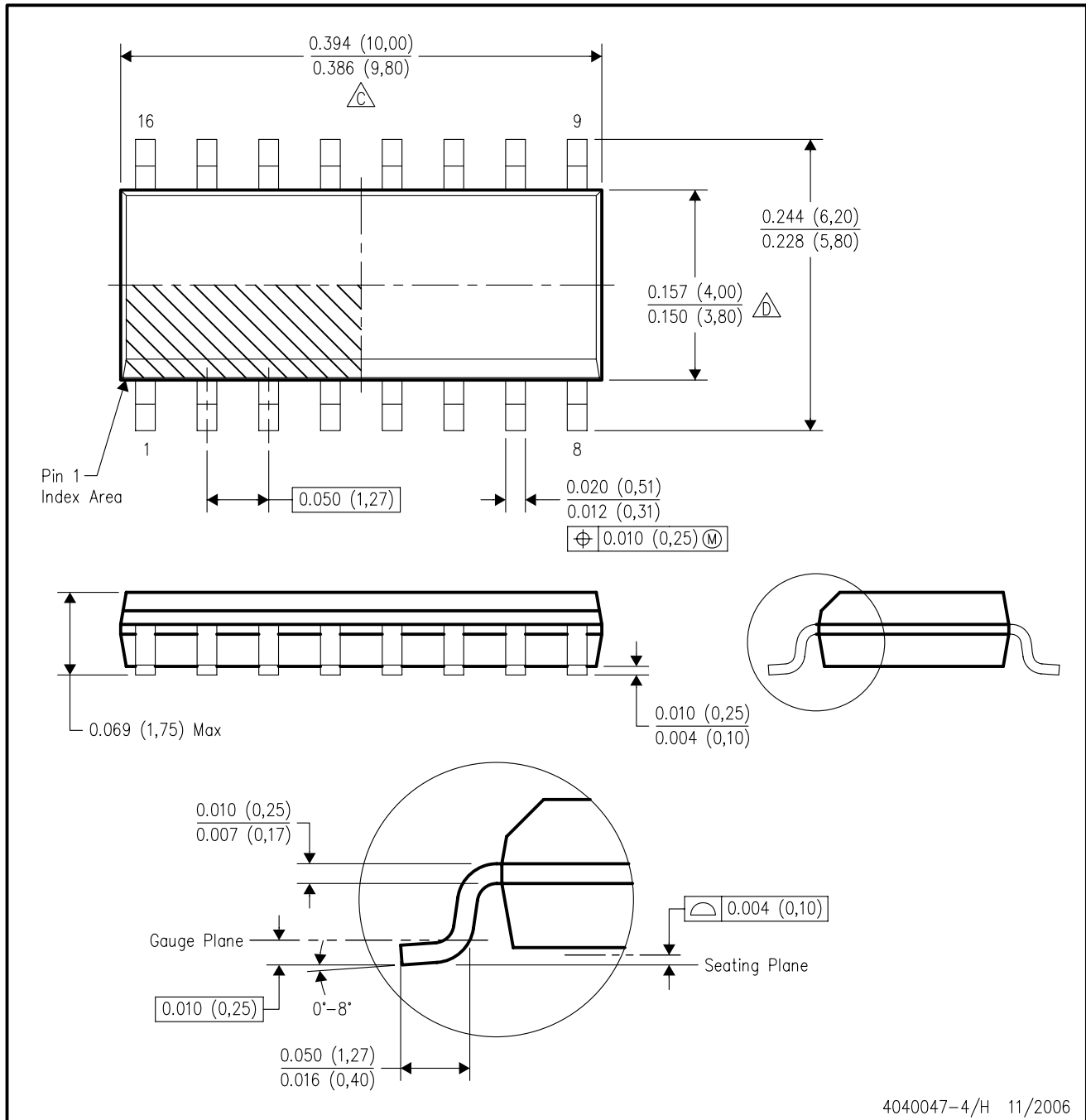
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



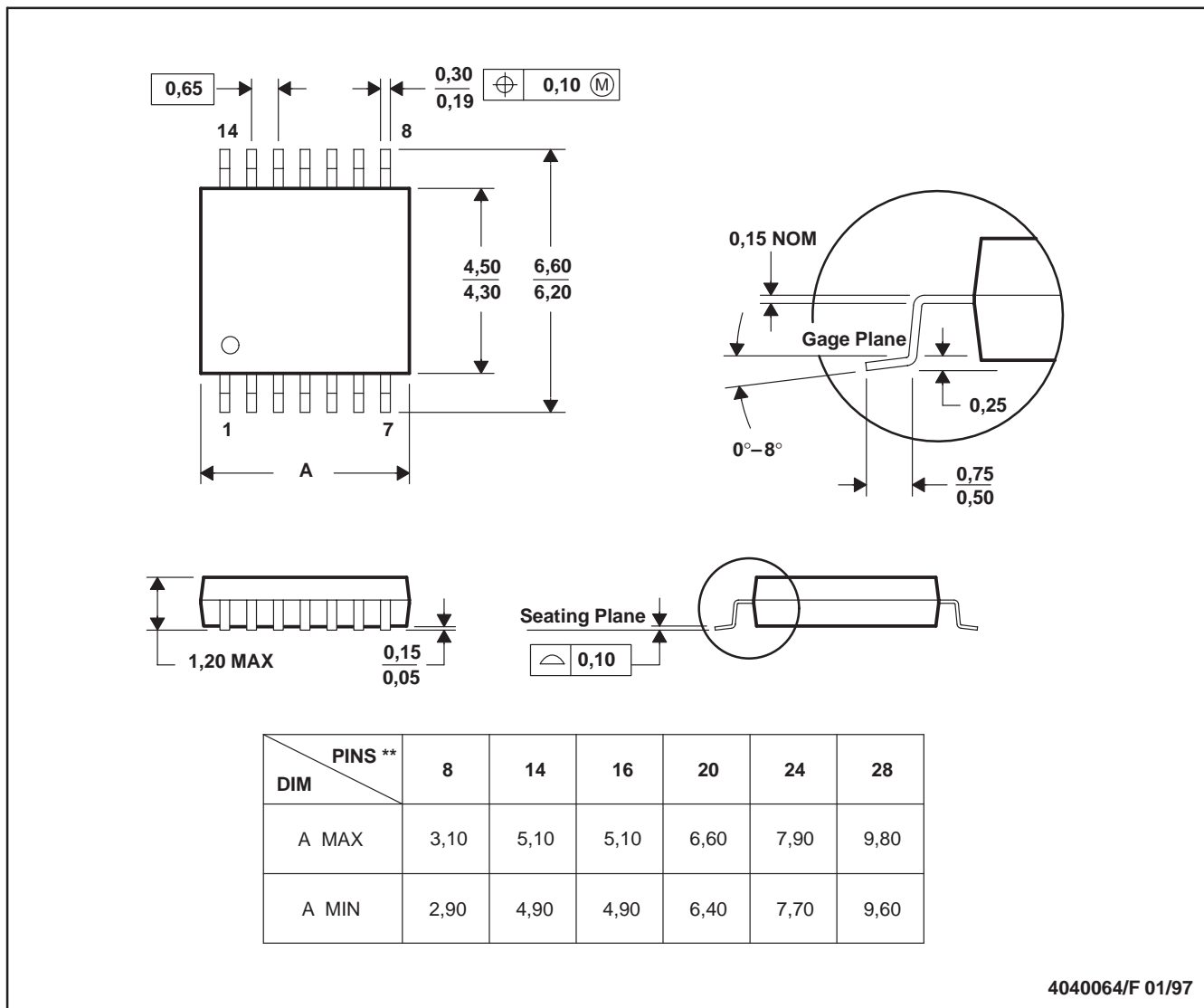
4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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