

T54LS109/109A
T74LS109/109A

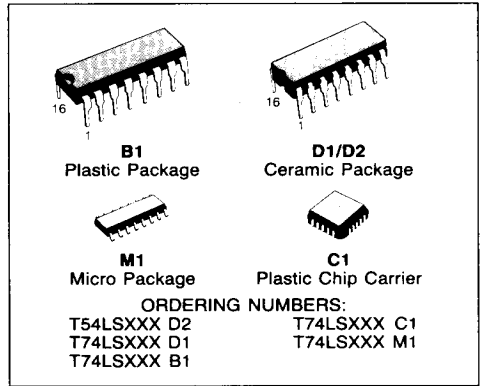


DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

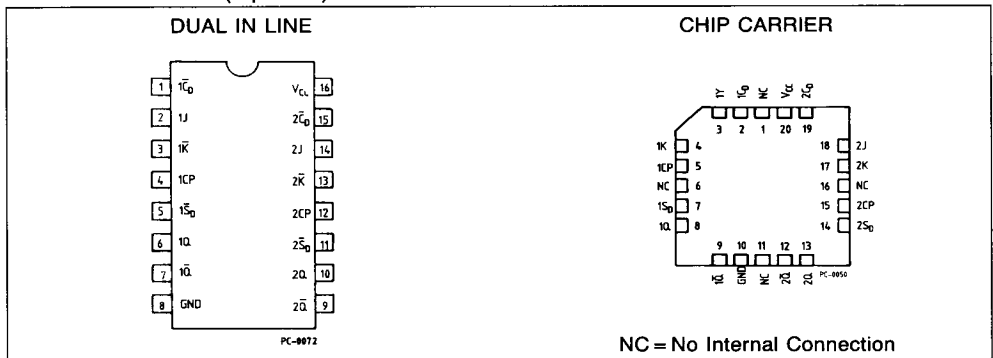
DESCRIPTION

The T54LS/T74LS109-109A consist of two high speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop by simply connecting the J and K pins together.

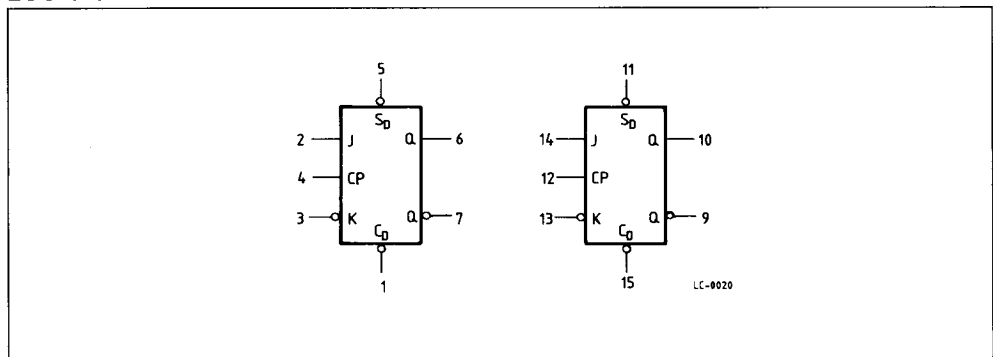
• VERSION "A" PRELIMINARY DATA



PIN CONNECTION (top view)



LOGIC SYMBOL





LOGIC DIAGRAM AND MODE SELECT TRUTH TABLE

LC-9021

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{C}_D	J	\bar{K}	Q	\bar{Q}
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
* Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	\bar{q}
Toggle	H	H	h	l	\bar{q}	q
Load "0" (Reset)	H	H	l	l	L	H

* Both outputs will be HIGH while both \bar{S}_D and \bar{C}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{C}_D go HIGH simultaneously. The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable, that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l,h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

ABSOLUTE MAXIMUM RATINGS

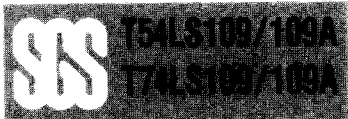
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	Input Voltage, Applied to Input	-0.5 to 15	V
V_O	Output Voltage, Applied to Output	-0.5 to 10	V
I_I	Input Current, Into Inputs	-30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS109/109AD2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS109/109AXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE T54LS/T74LS109

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units	
			Min.	Typ.	Max.			
V _{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V	
V _{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V	
		74			0.8			
V _{CD}	Input Clamp Diode Voltage			-0.65	-1.5	V _{CC} = MIN, I _{IN} = -18mA	V	
V _{OH}	Output HIGH Voltage	54	2.5	3.4		V _{CC} = MIN, I _{OH} = -400μA, V _{IN} = V _{IH} or V _{IL} per Truth Table	V	
		74	2.7	3.4				
V _{OL}	Output LOW Voltage	54,74		0.25	0.4	I _{OL} = 4.0mA I _{OL} = 8.0mA	V _{CC} = MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table	V
		74		0.35	0.5			
I _{IH}	Input HIGH Current	J, K Set, Clock Clear			20 40 80	V _{CC} = MAX, V _{IN} = 2.7V	μA	
		J, K Set, Clock Clear			0.1 0.2 0.4			V _{CC} = MAX, V _{IN} = 5.5V
I _{IL}	Input LOW Current	J, K Set, Clock Clear			-0.4 -0.8 -1.6	V _{CC} = MAX, V _{IN} = 0.4V	mA	
I _{OS}	Output Short Circuit Current (Note 2)		-20		-100	V _{CC} = MAX, V _{OUT} = 0V	mA	
I _{CC}	Power Supply Current			4.0	8.0	V _{CC} = MAX, V _{CP} = 0V	mA	

AC CHARACTERISTICS: T_A = 25°C T54LS/T74LS109

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
f _{MAX}	Maximum Clock Frequency		30	45		Fig. 3	MHz
t _{PLH}	Propagation Delay, Clock to Output			15	20	Fig. 3	
t _{PHL}					22	30	V _{CC} = 5.0V C _L = 15pF
t _{PLH}	Propagation Delay, Set or Clear to Output			10	15	Fig. 2	
t _{PHL}		CP = L			18		
t _{PHL}		CP = H			26	35	

Notes:

- 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at V_{CC} = 5.0V, T_A = 25°C



AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$
T54LS/T74LS109

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$t_{WCP(H)}$	Clock Pulse Width (HIGH)	18	12		Fig. 1	ns $V_{CC} = 5.0V$
t_W	Set or Clear Pulse Width	15	10		Fig. 2	
$t_s(H)$	Set-up Time HIGH, Data to Clock	18	12		Fig. 1	
$t_h(H)$	Hold Time HIGH, Data to Clock	0	-13			
$t_s(L)$	Set-up Time LOW, Data to Clock	20	13			
$t_h(L)$	Hold Time LOW, Data to Clock	0	-12			

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

T54LS/T74LS109A

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			-0.65	-1.5	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		$V_{CC} = \text{MIN}, I_{OH} = -400\mu\text{A}, V_{IN} = V_{IH}$ or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74	0.25	0.4		$I_{OL} = 4.0\text{mA}$ $I_{OL} = 8.0\text{mA}$ $V_{CC} = \text{MIN}, V_{IN} = V_{IL}$ or V_{IH} per truth table	V
		74	0.35	0.5			
I_{IH}	Input HIGH Current	J, K, Clock Set, Clear			20 40	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$	μA
		J, K, Clock Set, Clear			0.1 0.2		
I_{IL}	Input LOW Current	J, K, Clock Set, Clear			-0.4 -0.8	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	mA
I_{OS}	Output Short Circuit Current (Note 2)		-20			$V_{CC} = \text{MAX}$	mA
I_{CC}	Power Supply Current				8.0	$V_{CC} = \text{MAX}$	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$

T54LS/T74LS109A

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency		25	33		$V_{CC} = 5.0\text{V}$ $C_L = 15\text{pF}$	MHz
t_{PLH}	Clock, Clear, Set to Output			13	25		ns
t_{PHL}				25	40		

AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$

T54LS/T54LS109A

Symbol	Parameter		Limits			Test Conditions	Units
			Min.	Typ.	Max.		
t_w	Clock, Clear, Set Pulse Width		25			$V_{CC} = 5.0\text{V}$	ns
t_s	Data Set-up Time	HIGH	35				ns
		LOW	25				ns
t_h	Hold Time		5.0				ns

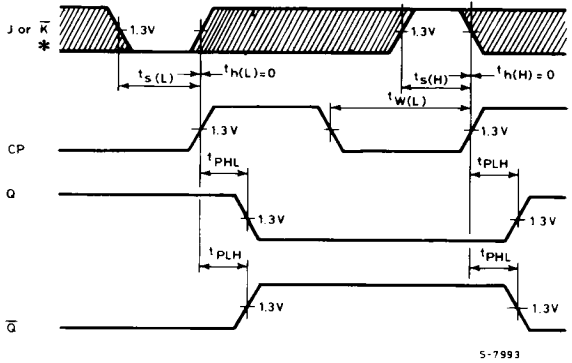
Notes:

- 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$



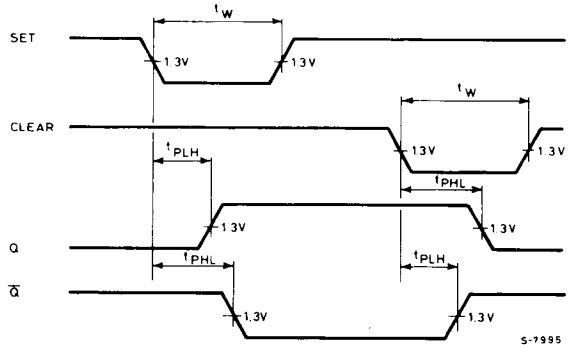
AC WAVEFORMS

Fig. 1 Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width



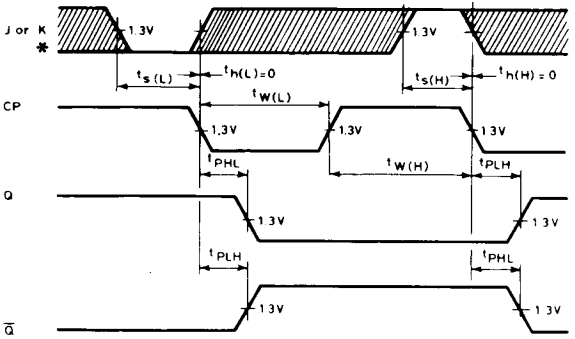
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Fig. 2 Set and Clear to Output Delays, Set and Clear Pulse Widths



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Fig. 3 Clock to Output Delays, Data Set-up and Hold times, Clock Pulse Width



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* The shaded areas indicate when the input is permitted to change to predictable output performance.