DUAL 4-BIT ADDRESSABLE LACTH

- SERIAL-TO-PARALLEL CAPABILITY
- OUTPUT FROM EACH STORAGE BIT AVAILABLE
- RANDOM (addressable) DATA ENTRY
- EASILY EXPANDABLE
- ACTIVE LOW COMMON CLEAR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

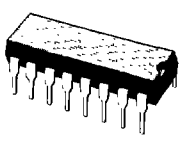
DESCRIPTION

The T74LS256 is a Dual 4-Bit Addressable Latch with common control inputs ; these include two Address inputs (A_0, A_1), an active LOW Enable input ($\overline{E}$) and an active LOW Clear input ($\overline{C}$). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

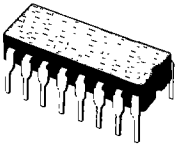
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{C}$) is LOW, all outputs (Q_0-Q_3),are LOW. Dual 4-channel demultiplexing occurs when the $\overline{C}$ and $\overline{E}$ are both LOW. When C is HIGH and $\overline{E}$ is LOW, the selected outputs (Q_0-Q_3), determined by the Address inputs. follows D. When the $\overline{E}$ goes HIGH. the contents of the lacth are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{C}$ = HIGH), changing more than one bit of the Address (A_0. A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{C}$ = HIGH).

PIN NAMES

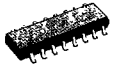
A_0, A_1	ADDRESS INPUTS
$\overline{D}_a$, D_b	DATA INPUTS
$\overline{E}$	ENABLE (active LOW) INPUT
$\overline{C}$	CLEAR (active LOW) INPUT
Q_{0a} - Q_{3a}. Q_{0b} - Q_{3b}	PARALLEL LATCH OUTPUTS



B1
(Plastic Package)



D1
(Ceramic Package)



M1
(Micro Package)

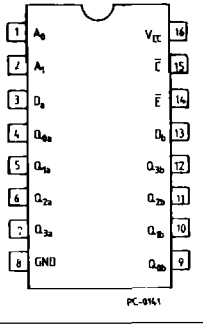
C1
(Plastic Chip Carrier)

ORDER CODES :

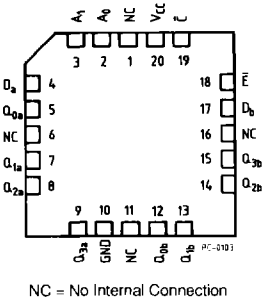
T74LS256 D1 T74LS256 C1
T74LS256 B1 T74LS256 M1

PIN CONNECTION (top view)

DUAL IN LINE

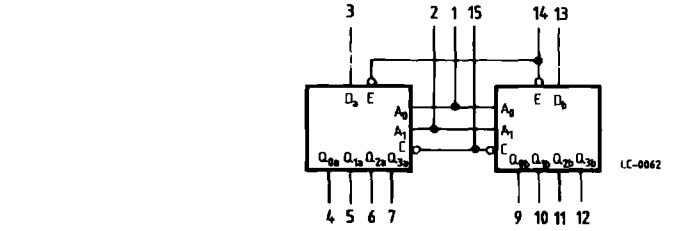


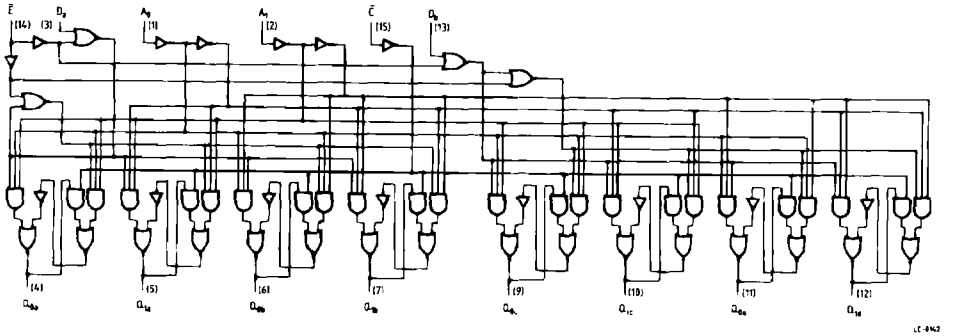
CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

MODE SELECTION

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4–Channel Demultiplexer
H	L	Clear

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS256XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

TRUTH TABLE

$\overline{C}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	Mode
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplexer
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q_{n-1}	Q_{n-1}	Q_{n-1}	Q_{n-1}	Memory
H	L	L	L	L	L	Q_{n-1}	Q_{n-1}	Q_{n-1}	Addressable Latch
H	L	H	L	L	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	
H	L	L	H	L	Q_{n-1}	L	Q_{n-1}	Q_{n-1}	
H	L	H	H	L	Q_{n-1}	H	Q_{n-1}	Q_{n-1}	
H	L	L	L	H	Q_{n-1}	Q_{n-1}	L	Q_{n-1}	
H	L	H	L	H	Q_{n-1}	Q_{n-1}	H	Q_{n-1}	
H	L	L	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	L	
H	L	H	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	H	

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current $\overline{A_0}$, A_1, $\overline{C}$, D_a, D_b, $\overline{E}$			 20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Input HIGH Current $\overline{A_0}$, A_1, $\overline{C}$, D_a, D_b, $\overline{E}$			 0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current $\overline{A_0}$, A_1, $\overline{C}$, D_a, D_b, $\overline{E}$			 - 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current		20	25	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_{PLH} t_{PHL}	Turn-off Delay, Enab. to Out. Turn-on Delay, Enab. to Out.		20 16	27 24	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Turn-off Delay, Data to Out. Turn-on Delay, Data to Out.		20 13	30 20	Fig. 2		ns
t_{PLH} t_{PHL}	Turn-off Delay, Addr. to Out. Turn-on Delay, Addr. to Out.		20 14	30 24	Fig. 3		ns
t_{PHL}	Turn-on Delay, Clear to Output		12	23	Fig. 5		ns

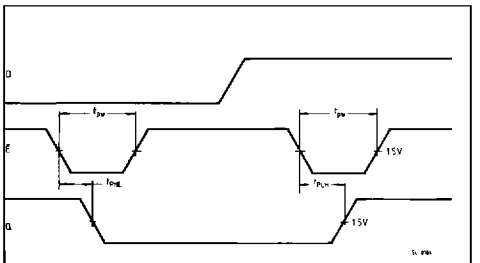
AC SET-UP REQUIREMENTS : $T_A = 25\ ^\circ C$

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
t_sH	Set-up Time HIGH, Data to Enable	20	13		V_{CC} = 5.0 V	Fig. 4	ns
t_hH	Hold Time HIGH, Data to Enable	0	– 7.0				
t_sL	Set-up Time LOW, Data to Enable	15	7.0				ns
t_hL	Hold Time LOW, Data to Enable	0	10				
t_sA-$\overline{E}$	Set-up Time, Address to Enable (note 4)	0	– 7.0		V_{CC} = 5.0 V	Fig. 6	ns
$t_w\overline{E}$	Enable Pulse Width	17	12		V_{CC} = 5.0 V	Fig. 1	ns

Notes : 4. The address to Enable Set-up Time is the time befor the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected
5: The shaded areas indicate when the inputs are permitted to change for predictable output performance.

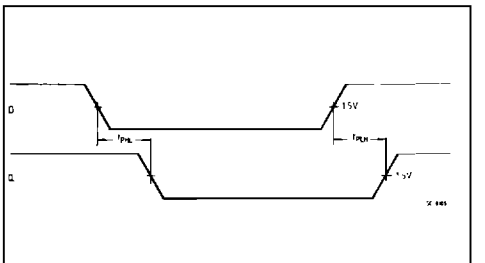
AC WAVEFORMS

Figure 1 : Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width.



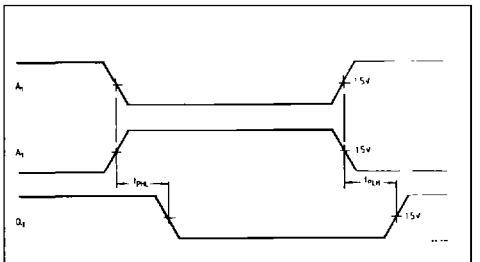
OTHER CONDITIONS : $\overline{C}$ = H, A = STABLE

Figure 2 : Turn-On and Turn-Off Delays, Data to Output.



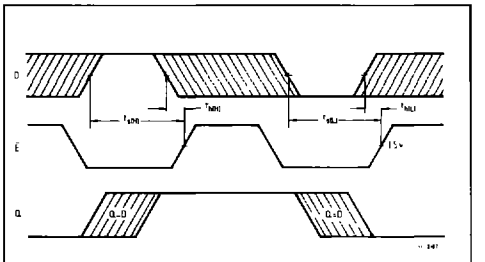
OTHER CONDITIONS : $\overline{E}$ = L, $\overline{C}$ = STABLE

Figure 3 : Turn-On and Turn-Off Delays, Address to Output.



OTHER CONDITIONS : $\overline{E}$ = L, $\overline{C}$ = L, D= H

Figure 4 : Set-up and Hold Time, Data toEnable.



OTHER CONDITIONS : $\overline{C}$ = H, A = STABLE

Figure 5 : Turn-On Delays, Clear to Output.

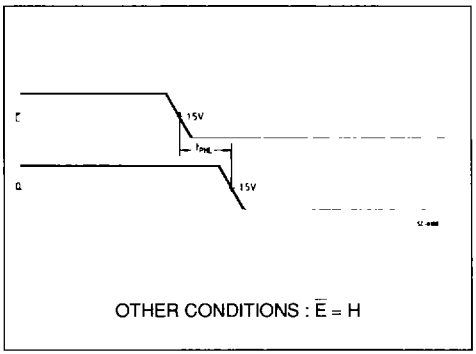


Figure 6 : Set-up Time, Address to Enable (see notes 4 and 5).