

SAA1061 Output Port Expander

Product Specification

Linear Products

DESCRIPTION

The SAA1061 is an NMOS output port expander circuit, which converts serial input data into parallel output information. The IC is used in combination with a microcomputer.

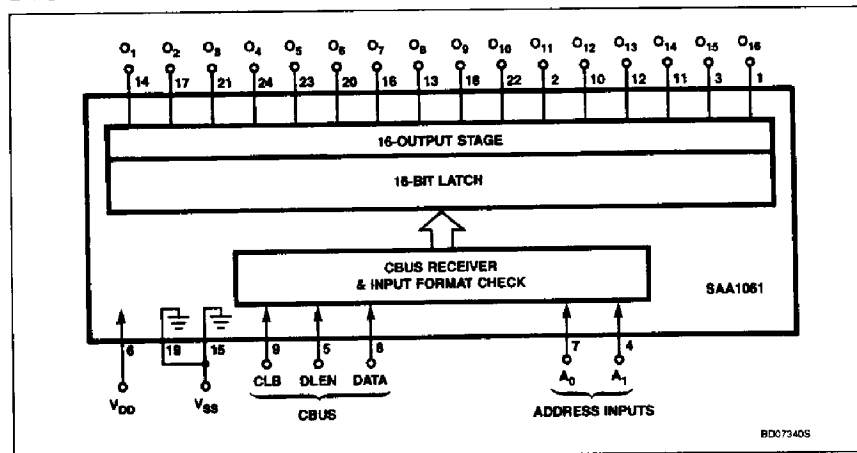
The SAA1061 is an addressable output port expander for use in microcomputer-controlled systems. It converts serial input data into parallel output information. The circuit comprises a CBUS receiver, logic to check input format, a 16-bit serial/parallel converter, latches and drivers for the parallel outputs.

The data is transmitted via the 3-line CBUS from the microcomputer. If the data transmission is valid, the data is transferred by a load pulse via the latch to the driver output. Each data transmission is checked for word length (18-bit) by the on-chip word format control circuitry. This allows different bus information to be supplied on the same bus lines for other circuits.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	-20°C to +80°C	SAA1061N

BLOCK DIAGRAM



The address inputs A_0 and A_1 determine four address possibilities. A data transmission only takes place if the programmed addresses correspond with the address bits S_0 and S_1 .

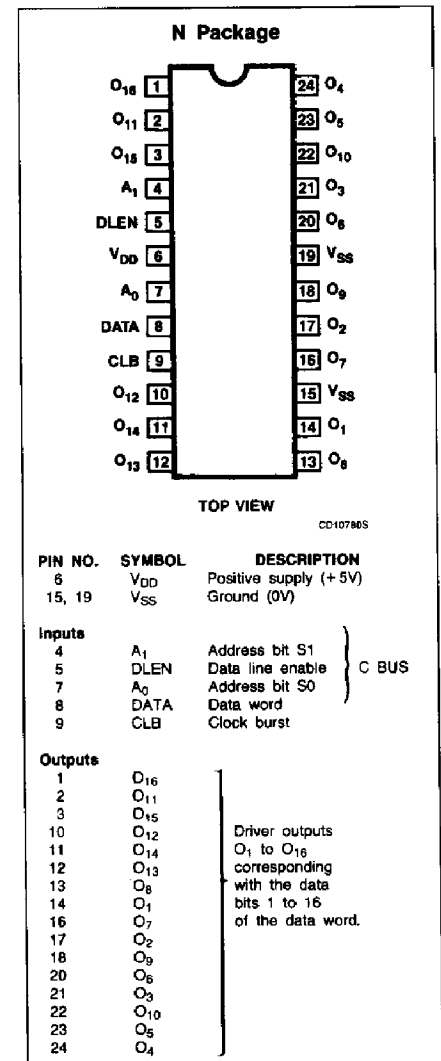
FEATURES

- Bus control for the selection of 18-bit words
- 16-bit latch and low-ohmic driver outputs
- Pin compatible with the SAA1060, except the SAA1061 has no duplex mode
- Address selection inputs; up to four SAA1061 circuits can be operated from a common CBUS

APPLICATIONS

- LED driver
- μP output port expander

PIN CONFIGURATION



Output Port Expander

SAA1061

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{DD}	Supply voltage range	-0.3 to +7.5	V
V _{IN}	Input voltage range	-0.3 to +15	V
±I _{IN}	Input current	10	mA
V _{OUT}	Output voltage range	-0.3 to +16.5	V
±I _{OUT}	Output current per output	20	mA
P _O	Power dissipation per output	7.5	mW
P _{TOT}	Total power dissipation per package	300	mW
T _A	Operating ambient temperature range	-20 to +80	°C
T _{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; V_{DD} = 5V; T_A = -20 to +80°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V _{DD}	Supply voltage		4.5	5	5.5	V
I _{DD}	Supply current				20	mA
Inputs CLB, DLEN, DATA, A₀, A₁						
V _{IL}	Input voltage LOW	T _A = 25°C	-0.3		0.8	V
V _{IH}	Input voltage HIGH		2.0		15	V
I _{IR}	Input leakage current	V _I = -0.3 to +15V			1	μA
Outputs O₁ to O₁₆ (open-drain)						
V _{OL}	Output voltage LOW	I _{OL} = 15mA			0.65	V
I _{OH}	Output leakage current HIGH	V _{OH} = 16.5V			20	μA
t _R , t _F	Rise and fall times	V _{OL} = 1.5V; V _{OH} = 13.5V			10	μs
C BUS timing						
t _R , t _F	Rise and fall times	} see Figure 1			2	μs
t _{SUDA}	Data setup time: DATA → CLB		400			ns
t _{HDDA}	Data hold time: DATA → CLB		250			ns
t _{SUEN}	Enable setup time: DLEN → CLB		400			ns
t _{SUDI}	Disable setup time: CLB → DLEN		600			ns
t _{SULD}	Setup time: DLEN → CLB (load pulse)		400			ns
t _{WH} , t _{WL}	CLB pulse width HIGH/LOW		450			ns

Output Port Expander

SAA1061

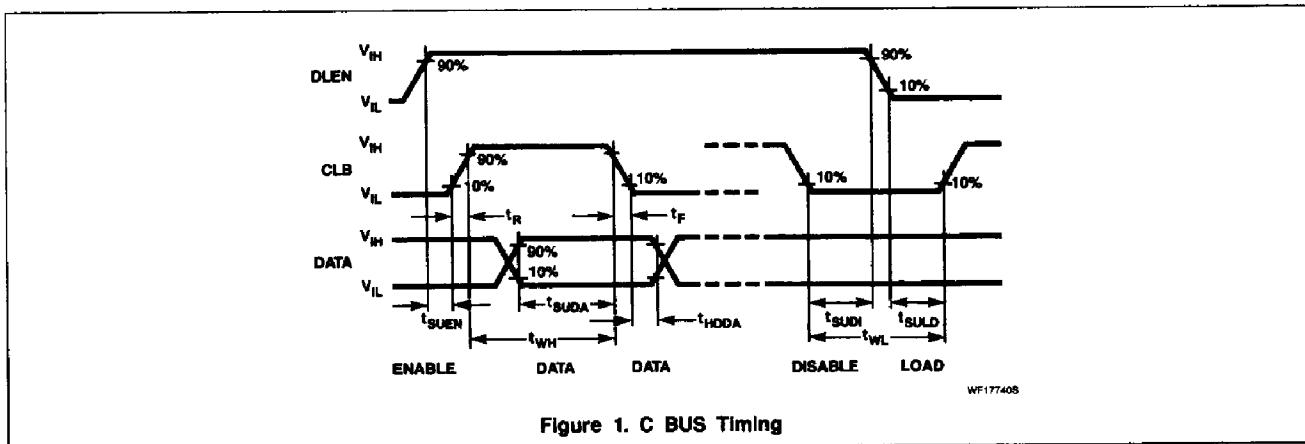


Figure 1. C BUS Timing

OPERATION DESCRIPTION

1. CBUS Transmission

The data words are entered via a serial CBUS interface. A clock burst of 18 clock periods is used to transmit the 16-bit data word, plus 2 identifier bits.

Serial data words, which are synchronized with the clock burst (CLB), are accepted if the

enable input DLEN is HIGH at the same time. Each transmission is checked for word length (number of clock pulses during DLEN is HIGH) and the address bits S0 and S1.

The valid data flag is only set if:

1. Word length is correct; 2 address bits and 16 data bits.
2. Address bits S0 and S1 correspond with A₀ and A₁.

Loading the information into the selected latch register is done by the load pulse (first clock pulse after the HIGH-to-LOW transition of DLEN) if the address bits correspond with A₀ and A₁. The load pulse or a new LOW-to-HIGH transition of DLEN resets the valid data flag. Only after the valid data flag is reset, will new data be accepted.

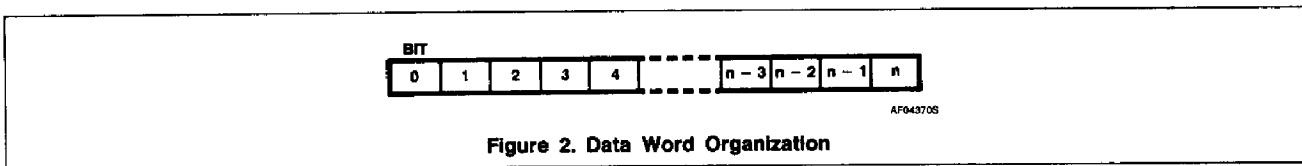


Figure 2. Data Word Organization

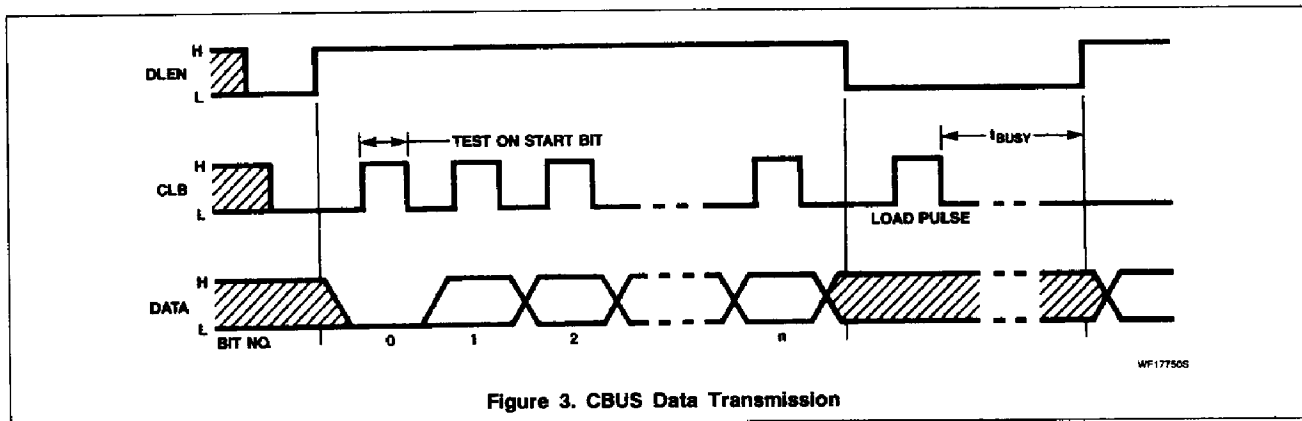


Figure 3. CBUS Data Transmission

Definitions to Figures 2 and 3:

- Word length: number of clock pulses during DLEN is active (HIGH); n + 1 bits = 18 bits.
- Bit number 0 is for the SAA1061 S0.
- Data bits: bit numbers 1 to n-1 (16-bits); bit no. n is S1.
- Load pulse: first clock pulse after DLEN returns to inactive (LOW).

2. Address Inputs A₀ and A₁

The 1st bit (bit S0) and the 18th bit (bit S1) of the data word are the address bits. Data is accepted only if the addresses correspond to the programmed addresses at inputs A₀ and A₁, that is for:

$$A_0 = S_0 \text{ and } A_1 = S_1.$$

3. Data Outputs O₁ to O₁₆

The outputs O₁ to O₁₆ correspond with the data bits 1 to n-1 (16-bits). The open-drain driver outputs (O₁ to O₁₆) are switched to ground (O_n = LOW), if the corresponding data bit is LOW.

4. Power-On Reset

The circuit generates internally a reset-cycle after switching on the supply and the outputs become high-ohmic (HIGH).